PDP-TV

SERVICE MANUAL

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PS42D8
PH50D8

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Note: This maintenance manual is intended only for the reference of the maintenance people. Please pay attention to the following points before carrying out the maintenance work.

Safety Instructions

Please read the “Points for attention for the Maintenance & Repair of PDP”and “Criterion for Identifying the Defects on Screen” as below, before inspecting and adjusting the TV set.

1. “Points for attention for the Maintenance & Repair of PDP”

To avoid possible danger, damage or jeopardy to health and to prevent PDP screen from new damage, the maintenance people must read the following carefully. If they ignore the following warnings, there will be deathful risks:

1). Screens vary from one model to another and therefore not interchangeable. Be sure to use the same type of screen in the replacement.

2). The operation voltage is approximately 350v for PDP module (including screen, driving circuit, logic circuit and power module). If you want to conduct maintenance work on PDP module when the set is in normal operation or just after the power is off, you must take proper measures to avoid electric shock and never have direct contact or touch with the circuitry of the working module or metal parts. That’s because within a short time relatively high voltage still remains on the capacitor of the driving part even after the power is off. Make sure to begin relevant maintenance operation at least one minute after the power is off.

3). Don’t apply on the module any power supply that is higher than the specification. If the power supply used deviates from the value given in the specification, there might be a possibility of leading to fire or damage to the module.

4). Never have operation or mounting work under unsuitable environment such as areas in the vicinity of water – bath room, laundry, water chute of kitchen – sources of fire, heat-radiation parts or direct exposure to sunlight. Otherwise there will be kickbacks.

5). In case foreign substances such as water, liquid, metal slices or others fall into the module carelessly power must be cut off immediately. Keep the module as it is and do not move anything on the module. Otherwise it might be possible to contact the high voltage or cause shock short circuit so that it may lead to fire or electric shock.

6) If there is smoke, abnormal smell or sound from the module, please cut the power off immediately. Likewise in case the screen doesn’t work when the power is on or during the operation, please also cut off the power at once. No more operation in this case.

7) Do not remove or plug its connection wire when the module is in operation or right after the power is off. That’s because there remains a relatively high voltage on the capacitor of the driving circuit. If there is a need to remove or plug in the connection wire, please wait at least one minute after the power is off.

8). Considering the module has a glass faceplate, please avoid extrusion by external force lest it

should cause glass breakage that may get people injured. Two people are needed in cooperation to move this module lest contingency takes place.

9). The complete TV set is designed on the basis of full consideration of thermal dissipation by convection, with the round hole on the top for heat emission. To avoid overheat, please do not have any covering on the hole during normal operation and never put it in the place where the space is narrow and in bad ventilation.

10). There are quite a number of circuits in PDP that are integrated ones. Please be on guard against static electricity. During maintenance operation be sure to cover yourself with anti-static bag and before operation make sure to have it sufficiently grounded.

11). There are a big number of connection wires distributed around the screen. Please take care not to touch or scuff them during maintenance or removing the screen, because once they are damaged the screen will fail to work and it's not possible to repair it.

12). Connector for the circuit board of the screen part is relatively fine and delicate. Please take care in the replacement operation lest it should get damaged.

13). Special care must be taken during transportation and handling because strenuous vibration could lead to screen glass breakage or damage on the driving circuitry. Be sure to use a strong outer case to pack it up before transportation or handling.

14). Please put it for storage in an environment in which the conditions are under control so as to prevent the temperature and humidity from exceeding the scope stipulated in the specification. For prolonged storage please cover it with anti-moisture bag and have them piled and stored in one place. The environmental conditions are tabulated as below:

Temperature	Scope for operation	0～50centigrade
	Scope for storage	-15～60centigrade
Humidity	Scope for operation	20%～80%
	Scope for storage	20%～80%

15). If a fixed picture is displayed for a long time, difference in its brightness and color may occur compared with movable pictures. But it doesn't show any problem and the reason is that there is reduced density of fluorescent powder in the former. On the other hand, even if changes take place in the picture, it can keep its brightness for a period of time (several minutes). It's a feature inherent with plasma and it's not abnormal. However please try as much as possible to avoid showing a still picture of high brightness for a long time during operation.

16). As a digitalized display devise, this module is provided with error diffusion technology and the

gray scale and false enhancement of contour can be displayed by reusing of sub-field. As compared with cathode ray tube, it can be found in the moving picture that at the brim of the face of a person there are some wrong colors.

17). During the display of graph (indicating the gradual change in brightness horizontally or vertically) resulting from gray scale test it can be found that the brightness for the two adjacent levels is uneven. This is caused by the reuse of sub-field, the display of load rectification and the eletrolyzation.

18). The screen front plate is of glass. Please make sure that the screen has been put in place during erection. If it is not in place before the erection begins it may lead to screen crack or breakage.

19). Make sure the screw used in the mounting of the screen is of the original specs lest it should cause damage to the screen due to mismatch. Special care should be taken not to use too long or too big screw.

20). Care must be taken to guard against dust during assembling or dismantling, especially to avoid dirt from falling in between the screen and the glass lest it should harm the receiving and viewing effect.

21). There is piece of insulator stuck on the rear chassis corresponding to the power supply board. It is used to isolate the cool part from the hot part. Please take care to keep it intact lest it should become a potential safety trouble.

22). In addition to plasma screen, the glass is a part of high value. It has such functions as anti-radiation, adjustment of color temperature etc. Please handle it carefully.

2. "Criterion for Identifying the Defects on Screen"

The PDP produced by our Company at present uses the following criterion for identifying the defective points:

2.1、Model PS－42D8:

There may appear three kinds of defective points for this model as shown in Fig.1, i.e.,

bright spot (remain bright); dark spot (non-illuminating); flickering spot (continuously flickering).

However they should not exceed the specification as in table 1. Otherwise the product shall be deemed as sub-standard.

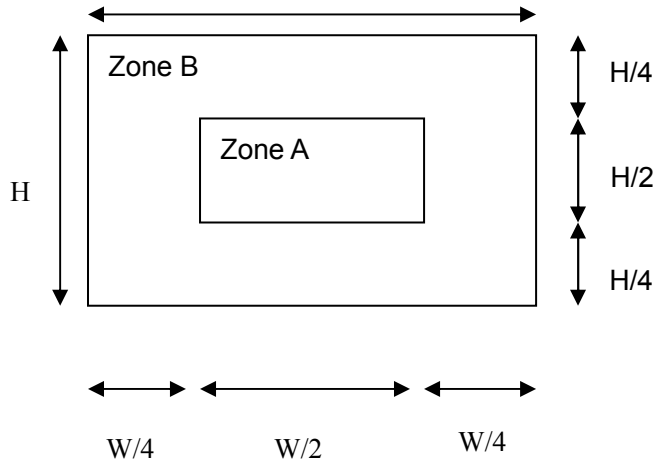


Figure 1 Defective Points

Table 1 Criterion for Three Kinds of Defective Points

Kind	Area A	Area B	Remark
Dark spots	No more than 2	No more than 8	Total number of defective points in A and B shall not exceed 8. The distance between two defective points shall not be shorter than 15mm.
Bright spot	No more than 1	No more than 2	
Flickering spot	No more than 1	No more than 2	

2.2. Model PH－50D8:

There may appear three kinds of defective points for this model as shown in Fig.2 -- bright spot (remain bright); dark spot (non-illuminating); flickering spot (remain flickering). However they should not exceed the specification as in table 2. Otherwise the product shall be deemed as sub-standard.

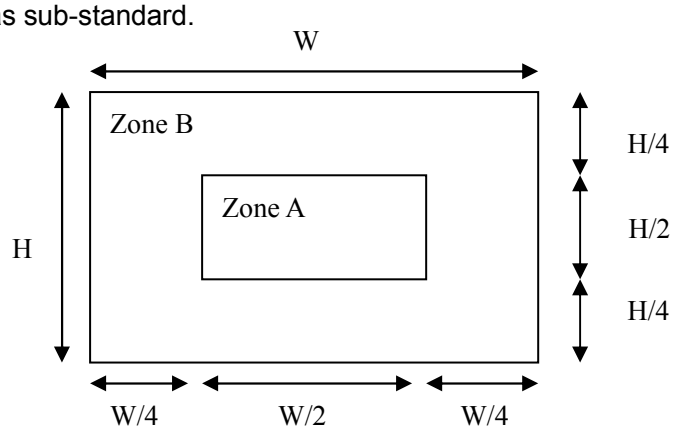


Figure 2 Defective Points

Table 2 Criterion for Three Kinds of Defective Points

Item	Kind	Area A	Area B	Remark
1	Dark spots	No more than 4	No more than 10	Total number of defective points in A and B shall not exceed 14. The distance between two defective points shall not be shorter than 10mm.
2	Bright spot	No more than 1	No more than 3	
3	Flickering spots	No more than 1	No more than 3	

Method of Debugging

For Models PS-42D8 and PH-50D8, the debugging part lies only in the white balance adjustment. Nothing else should be adjusted and the maintenance software supplied for after-sale purpose has normally shielded the value of white balance i.e., no more adjustment is needed when upgrading the software. In case of special circumstances where the main board is replaced following method can be adopted:

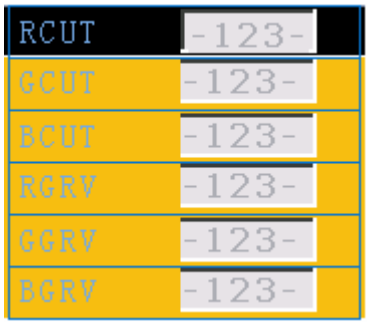
1). The white balance adjustment is made respectively in three ways - TV/AV、VGA、YpbPr. First adjust TV/AV, then VGA and YpbPr at the last

2). Select corresponding channels respectively. After successively press the keys on the production plant's remote control (the key at the right hand lower corner doesn't show up), go on to press the left key, right key, confirmation key on the small keyboard one by one and then it's possible to enter the menu set up in the plant.

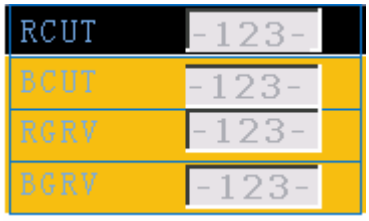
3). Use the right key to select and calibrate the menu. The white balance adjustment and YpbPr white balance adjustment are for the purpose of white balance adjustment. For the white balance adjustment of TV/AV and VGA it's OK just directly adjust the first item whereas for YpbPr adjust the second item.

4) For the white balance adjustment of TV/AV and VGA: select the item of "white balance adjustment" from the menu. When it's entered (as shown in the fig. Below), keep RCUI immovable and adjust GCUT and BCUT so as to adjust the white balance of the dark area. For the adjustment of white balance of the bright area, keep RGR immovable and then adjust GGRV and BGRV. Repeat the above steps several times until the picture is normal in white balance.

For the white balance adjustment of YpbPr: select the item of "white balance adjustment" from the menu. When it's entered (as shown in the fig. Below), adjust RCUT、BCUT and it's done.



5).Note: Except for the two items in the plant setup menu as above used for the white balance adjustment and the items 5,6,7 (for test of pattern, color collocation and degree of pure gray) in the calibrated menu that can be used to shoot trouble, no adjustment should be made for the other items. Otherwise it may cause abnormality to the set. The internal test signal of PW181 can be used for troubleshooting.



Method of software upgrading

The plasma TV models PS-42D8 and PH-50D8 launched by our company are equipped with RS-232 interface for upgrading that is carried in the steps below:

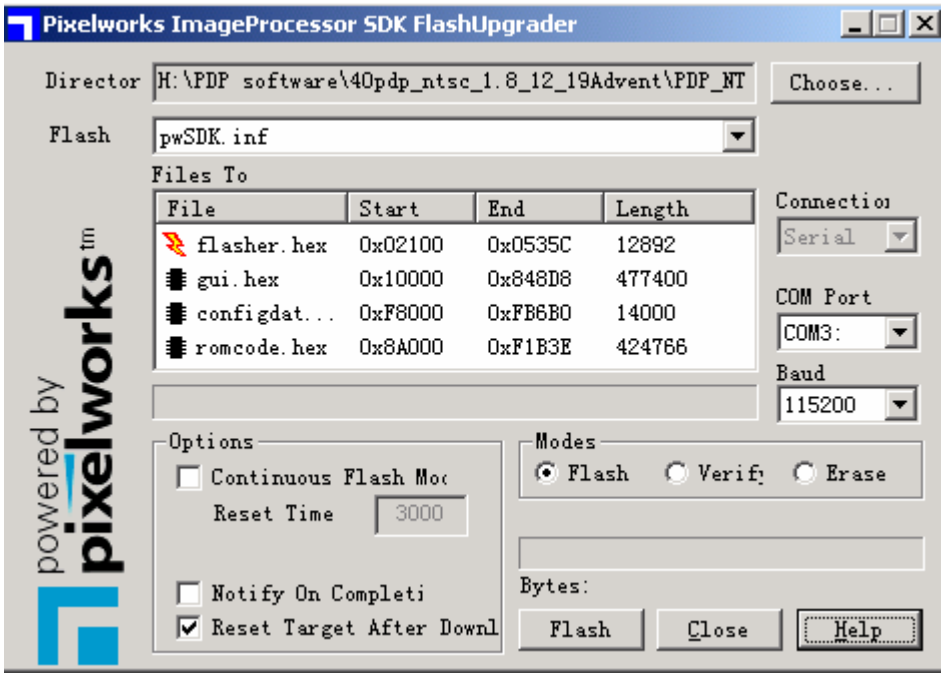
A. Select a connection wire of serial port (see the figure below) which is required to have a notch on its both ends and also the pins 2 and 3 on the two ends are cross-connected.

B. Use the serial port connection wire to connect PC with PDP and set PDP to the off position.

C. Open the folder of the upgrading software and double click the FlashUpgraderNT (on condition of window 2000/XP/NT)

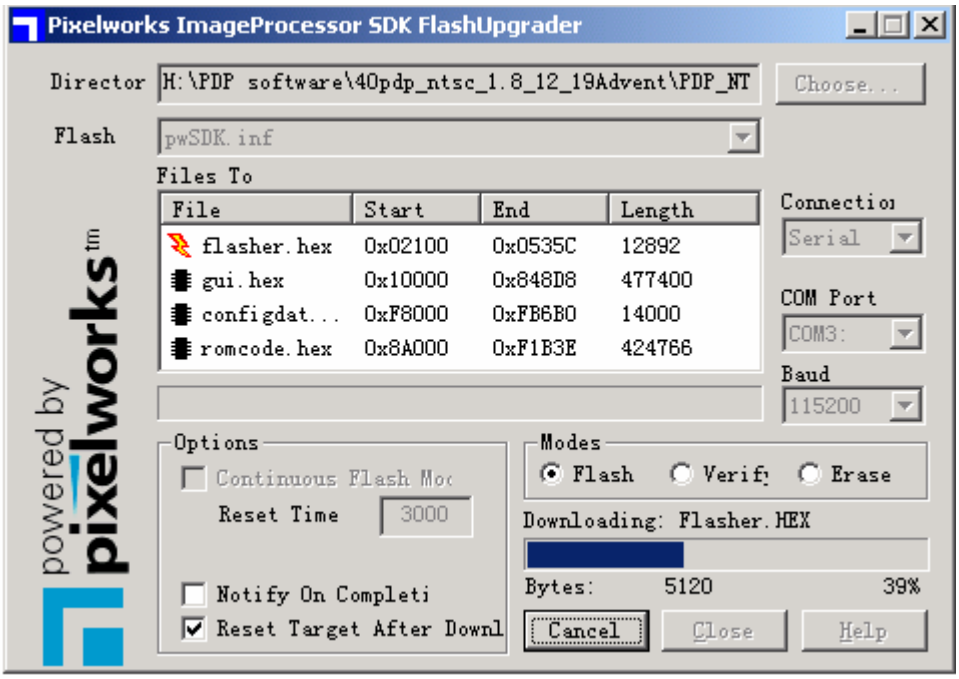
or the FlashUpgrader (on condition of window 98)

After running the programs the following interfaces will appear:



Based on the features of computer set up the serial port (COM Port) and select corresponding serial port (if it's not possible to burnt-write other serial port can be used instead). Baud-select 115200 and then select Reset Target After Download. Hit flash press button and it's ready to operate. For the setup of other items please refer to the figure above (already defaulted by the system so it's normally unnecessary to alter)

A. Switch on PDP and it begins to run the burnt-write program;



B. Once it's over with burnt-write, the cancel pushbutton will become flash. Switch off the main power and then to switch on the TV set again.

Note: Do not switch the power or the set off in the course of burnt-writing. Otherwise it may result in the inability of the flash to burnt-write again.

Briefing on the operation principle of the plasma TV series PS-42D8

Plasma plane screen technology represents the state-of-the-art and it's also the best choice for high quality picture and large purely place screen. Plasma display screen PDP is a display unit employing gas discharge. This screen uses plasma tube as its light emission component. The faceplate (panel)of PDP consists of many image elements (plasma tubes) for example, the 42"pdp now on the market consists of 852*480 image elements. Each image element in turn consists of three kinds of image sub-elements. Each image element is actually a plasma tube. These tubes are present respectively in red, green and blue colors, as shown in fig. I. Each small chamber that corresponds to each plasma tube is filled with neon and xenon gases. After applying high voltage between the plasma electrodes, the gases in the small chambers of the plasma tubes sealed in the two layers of glass will produce ultraviolet so as to excite the three basic color (red, green and blue) fluorescent powder to emit visible light. Each plasma tube acts as an image element. From the composition of these image elements in different brightness, darkness and colors result the pictures and images of various grays and colors, which is very similar to the light emission of display tube. Plasma technology is obviously different form other display methods and is more advanced in structure and formation. Its working principle is similar to normal daylight lamp. The TV color picture is composed of the light emitted from various independent fluorescent powder image elements and therefore the picture is fresh and gaily colored, bright, clean and clear. Furthermore the most outstanding feature of plasma TV is that it can be made super thin and it's easy to make TV sets of more than 40" with completely plane big screen but in thickness less than 100 mm (Our Model PS-42D8 is only 79mm thick and it's the thinnest in the market at present.)

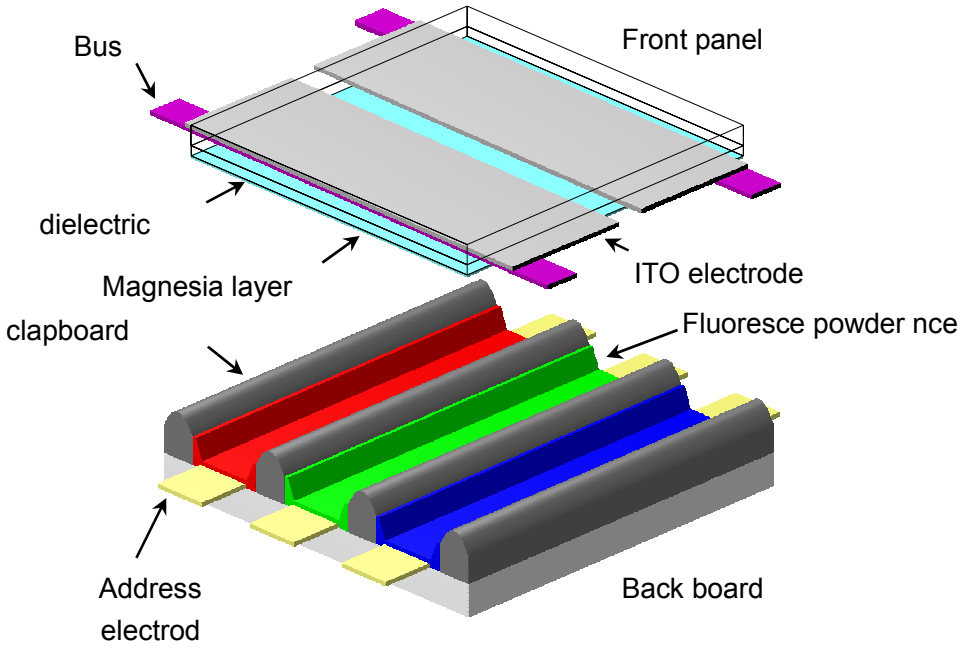
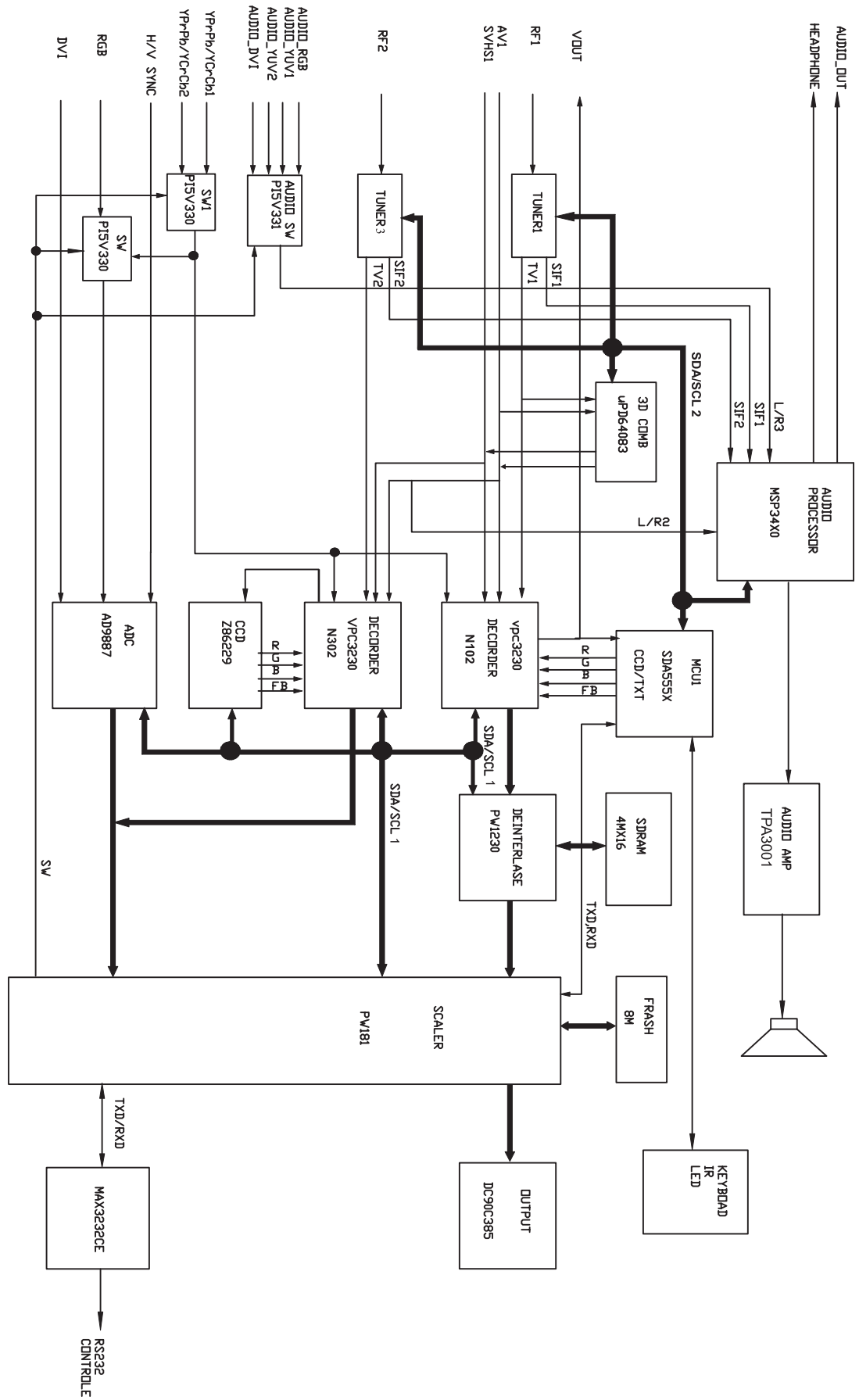


Figure I Structure of Image Element

Plasma TV model PS-42D8 series of XOCECO is designed and developed by XOCECO itself. In terms of the main CMOS chip this series of TV set employs PW181 made by Pixelworks Company.

1、 The block diagram of the complete TV set is as follows:



Among which:video decoder:VPC3230 Non-interlace conversion:PW1230
Ad conversion and DVI interface :AD9887 Audio treatment:MSP3440
Sound power amplification:D type power amplification of TI : Tpa3001
3D Y/C separation:uPD64083
CCD/V-CHIPdecoder:Z86229（For North America only）

Below is a short introduction to the basic work process flow of model PS-42D8series:

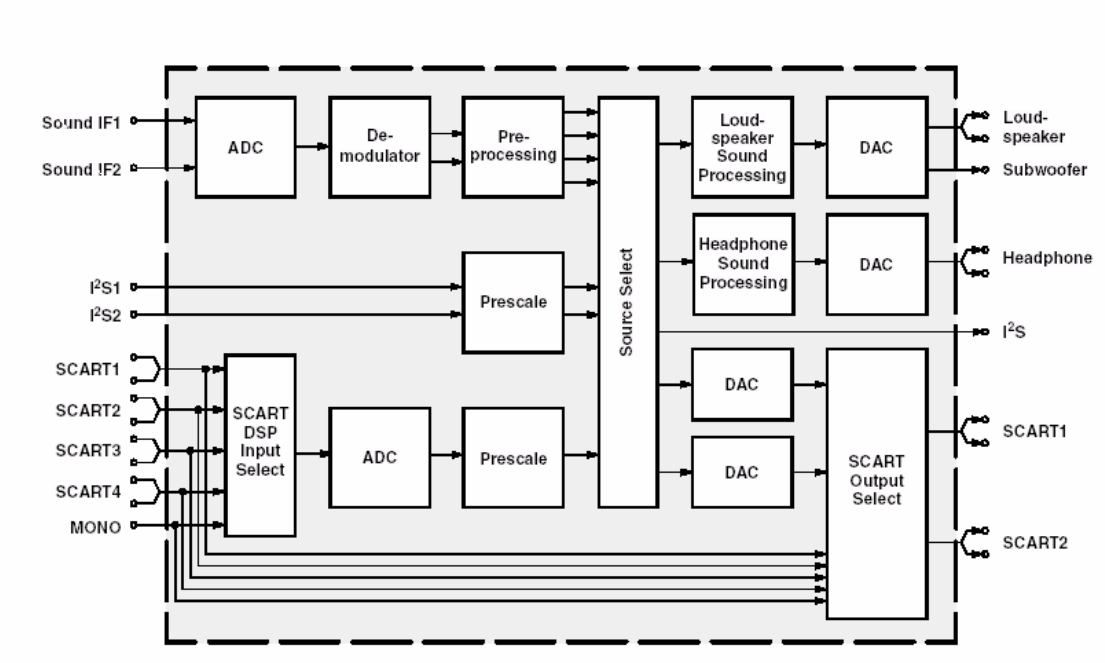
This TV model is based on dual MCU control of which the main MCU is PW181（N501, taking care of the operation of various chips (including image treatment, channel switching, image display etc.), infra red remote control receiving, the standby control, the control of auxiliary CPU, menu display, debugging of picture effects and other major functions. The auxiliary CPU is SDA555X（NM5, which is responsible for sound treatment (including volume adjustment, control of alt and base sound, stereo decode), station searching control, push button, separation of 3D Y/C (valid only for system N) as well as the CCD/V-CHIP decoding for the text for oversea sale TV sets etc. Connection between two MCU is made by means of three pins of X708, i.e., INT (interruption), S1(RXD), S2（TXD）

2.Volume of sound

This model employs double integrated tuner (including high frequency and medium amplification circuits). The signal received by antenna is fed to the main tuner, TUNER1, which contains a high frequency distributor, from which RF signal is shunt to supply to TUNER3 for use. Pin 14 of TUNER1 is for the power supply of high frequency distributor (+5v). Tuners are controlled by auxiliary MCU NM5 （SDA、SCL）to select proper channel and carry out correct switching of systems. After high amplification and medium amplification decoding, video signal and audio signal are output. The output signal of TUNER1 is fed into decoder N102 as the display of main picture whereas the output signal of TUNER3 is fed into decoder N302 as the display of the auxiliary picture for dual picture. Audio signal is directly fed into audio frequency processor NM2 MSP3440. At the same time dual way tuners all send their medium frequency signal of the second sound to NM2 for treatment (used for decoding of stereo or automatic sound volume control). NM2 is provided with the switching over device for audio frequency channels. Audio input of VGA/DVI/YprPb of the main board, after the switching-over as selected by N3, is fed together with the audio signal of TV and AV into NM2, where switching over is selected. The selected audio frequency signal is made use of in the following three ways. One way is, after being subjected to the control of volume and alt and base sound, fed separately through left and right sound channels into sound power amplifier TPA3001 for amplification. Then it is fed into the loudspeaker for sound reproduction. Another way is also fed separately through left and right sound channels into earphone power amplifier NM9 TDA7053 for amplification before being output to earphone socket for listening, of which the volume is controlled by PWM signal produced by pin 50 of NM5.

The remaining way is output through video board as AV out..

The block diagram of MSP3440 is as follows:



2, 3:SCL、SDA，for the control of IC operation;

27,28:output to the right and left channel of sound power amplifier;

33,34:right and left channel of earphone sound;

36,37:AV OUT right and left channel of sound;

47,48:right and left channel of sound fed from main board;

50,51:AV IN right and left channel of sound;

53,54:right and left sound channel of sub-channel TV;

56,57:right and left sound channel of main channel TV;

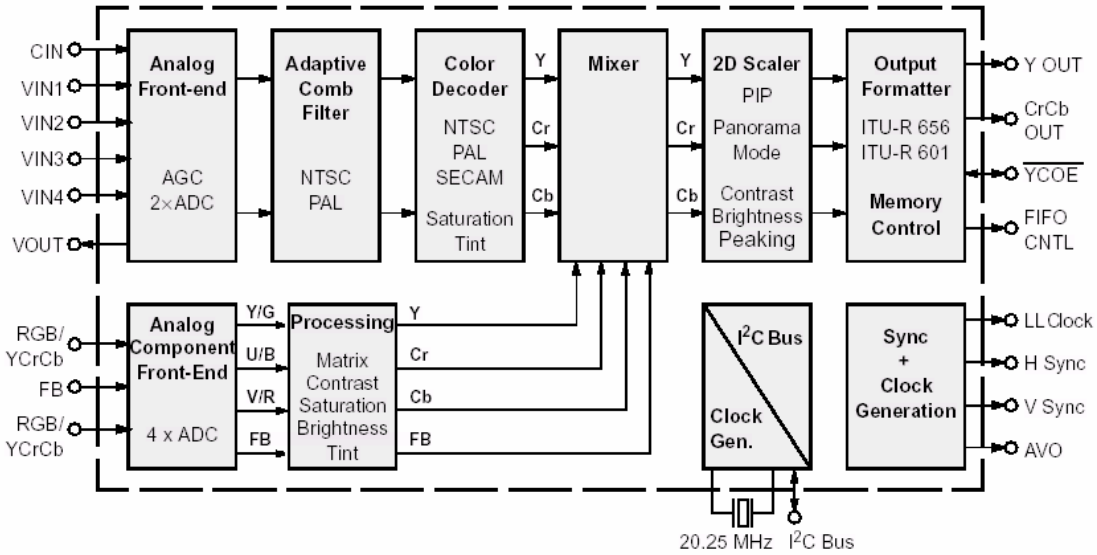
67,69:SIF input of main and sub channel TV

Sound power amplifier TPA3001 is an amplification of mono-channel high efficiency D type power. Under the condition of no heat dissipation its output power can be as high as 20 w. It has the functions of over current and overheating protection. Automatic protection comes in when the input to the ground is short-circuited. Then output is stopped. After the removal of short circuit, switch the set again and it restores to normal. Therefore if the set becomes soundless due to the short circuit caused in carelessly pulling out or plugging in the audio frequency wire (it is certainly not recommendable to do so), just switch it on again and no big deal.

3. Picture and image:

Y signal of AV and SVHS shares the same channel. SVHS has priority. Identification of terminal S is determined by electric level SID fed from SVHS socket to NM5. When the electric level of SID is of high value, the system is identified as SVHS. Signals from TV or AV and YCRCB are altogether fed into digital decoder VPC3230 (sent separately in two ways to N102 and N302). Channel switching is carried out. They are decoded into 16bit CCIR601 signal to be fed into the processor of lower level for treatment. VPC3230 mainly functions to switch over channels, separate Y/C
of 4 lines, decoding of colors and adjustment of picture effect.

3．1 The block diagram of VPC3230 is shown below:



In which: Pin 71 is used for the input of C signal of SVHS;

Pin 72 VIN1 is used for the input of Y signal of CVBS or SVHS of AV;

Pin 73 VIN2 is used for the input of TV signal;

Pin 75 VIN4 is used for the input of Y signal of YCRCB to synchronously identify YCRCB.

Main channel: The digital YCRCB signal in the format of CCIR601 after being decoded in N102 is fed into non-interlace processor N204 PW1230 for treatment from alternate-line into non-interlace. VD1_CLK,VD1_HSYNC VD1_VSYNC, VD1_ACTIVE and VD1_FIELD sent from VPC3230 is used as a key signal to identify modes. If certain channels become abnormal the corresponding pictures will also become abnormal. In addition to the function PW1230 has to process the signal from alternate-line into non-interlace, it can also function to enhance the picture and convert the movie modes 3:2/2:2. The adjustment of brightness and contrast of the main channel is performed by this chip whereas the adjustment of chroma and definition is performed by N102. The digital 24 bit RGB signal output from PW1230 after treatment is fed into V PORT of N501 PW181 for further processing. The signals of VCLK (clock)、VVS（field synchronization）、VHS（line synchronization）、VPEN（enable signal）are the basic reference for the image processing of lower level.

For TV set of mono N system, this series has an additional 3D Y/C separation function in the main channel, which is performed by ND02 Upd64083 so as to enhance the quality of the image.

In this case the signal flow process of the main channel is different. Video signal and AV/SVHS signal sent from TUNER1 first undergo switching in the switch circuit ND01, then are fed into ND 02 for separation of brightness from color and output as signal Y and C. For N102, no matter whether it's TV or AV/SVHS, finally the signals are all fed in the form of Y/C into the input port of VIN1and CIN. Yet the setup for the software is somewhat different.

The decoding for the text of main channel or CCD/V-CHIP is performed by auxiliary CPU. Video signal is directly fed to pin 12 of NM5 for decoding. The decoded text or CCD/V-CHIP signal is output in the form of R, G, B, FB and fed into N102 for character superposing.

Sub-channel:

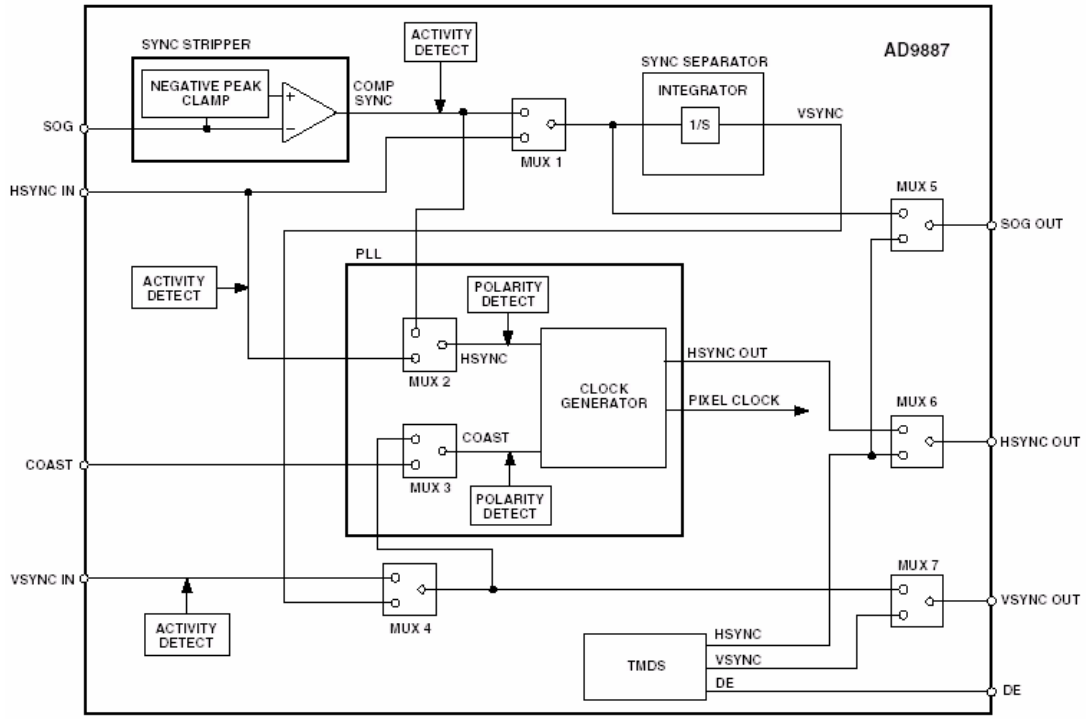
Signal CCIR601 after being decoded in VPC3230 is directly fed into PW181 的G PORT where direct processing is carried out by PW181. The non-interlace conversion in this channel is performed by the non-interlace processor inside PW181. Relatively speaking, the efficiency of the internal non-interlace

processor of PW181 is lower than that of PW1230. Therefore when displaying dual picture the main picture effect is better than that of sub-picture. The adjustment of brightness, contrast, definition and chroma is performed by N302.

The decoding of CCD/V-CHIP in this channel is specially performed by 21 line decoder N301 Z86229. The decoded information is superposed onto the image in N302 also in the form of R, G, B and FB.

For VGA and YPRPB, after the selection in N1 YPRPB1 and YPRPB2 are fed together with N402 for channel selection. The selected signal is fed into the ADC part of N403 AD9887 for A/D conversion so as to produce 24 bit digital RGB signal to be fed into the G PORT of PW181. The line and field synchronous signal of VGA is directly fed into N403 whereas The line and field synchronous signal of YPRPB is obtained after synchronous separation of Y signal of SOGIN
in AD9887 (This signal is input to N403 pin 108).

Synchronous switching device is shown in the following figure:



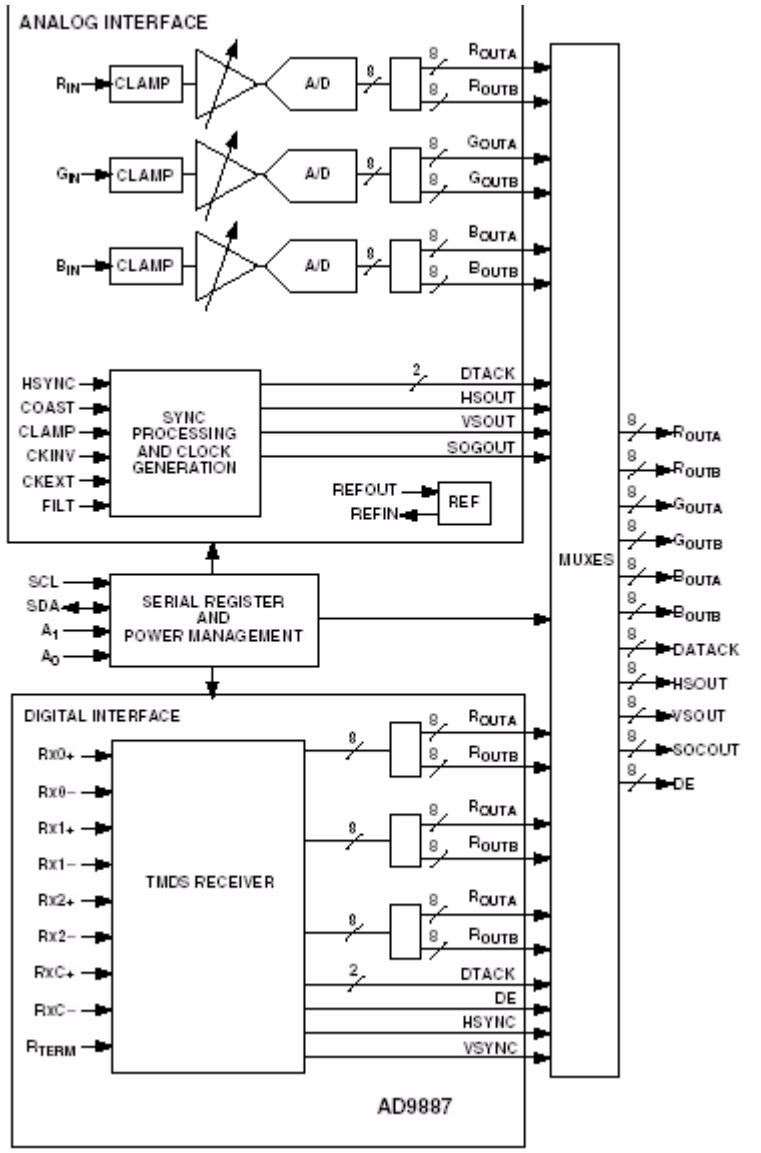
AD9887 is also provided with DVI input port. The DVI input signal is converted into 48 bit digital RGB signal and sent to G PORT of PW181 for processing. The selection from DVI and VGA/YPRPB is performed by AD9887.Certain organizations for the oversea sales of this TV series have been equipped with the capability to decode HDCP. PORTA4 and PORTA5 of PW181 verify the password (cipher key) through bus line with broadcast equipment. Each TV set has its own independent password, which is stored in EEPROM.

The mode identification of VGA or YPRPB is performed by PW181. The identification process is :

When selecting channel signal input PW181 presets the synchronous selection of AD9887 so that it can directly output the required synchronous signal for direct feeding to PW181. The synchronous signal format is identified inside PW181. By making cross-reference with the format table pre-stored inside a most similar format is obtained. Then the parameters of this format are called for use in setting up the parameters for modular conversion so that it is optimized. At the same time the conversion coefficient of

SCALER is confirmed.

3.2. Block diagram of AD9887 is shown below

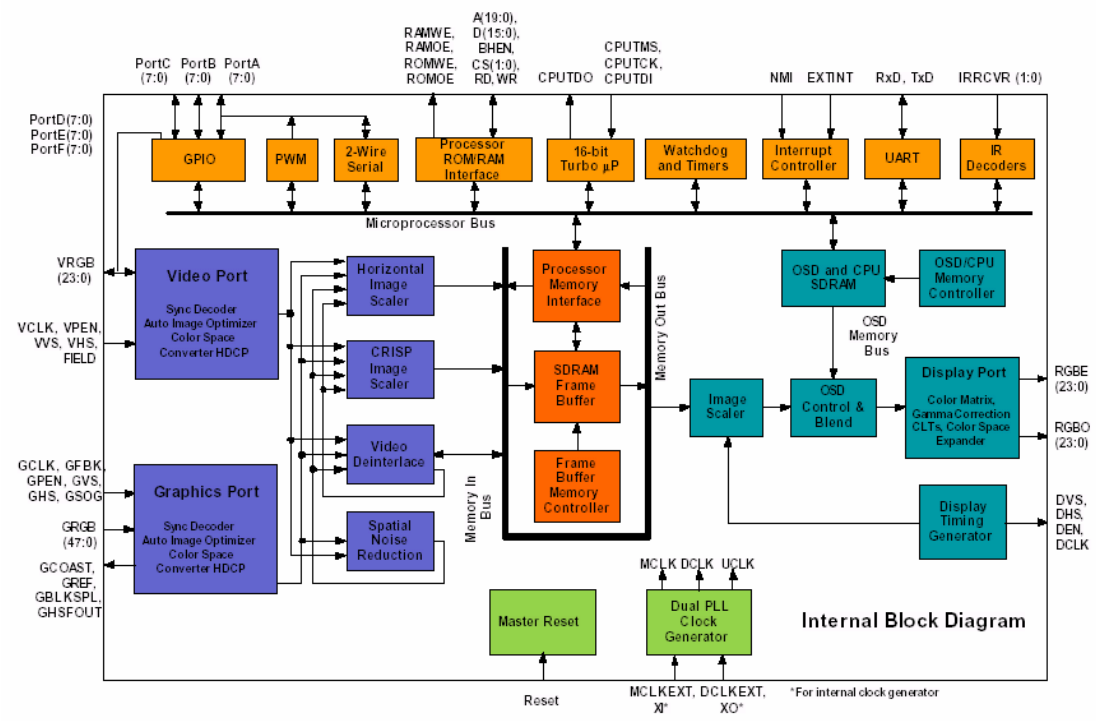


Finally the video signals of different channels are sent respectively to V PORT and G PORT of main processing chip PW181 for processing. PW181 has such processing capabilities as “picture out of picture”, “picture in picture”, “multiple pictures”. So long as the signals come respectively from V PORT and G PORT, they automatically become “picture out of picture”, “picture in picture”. PW181 has the function of SCALER, which means it can conduct format conversion for the input signals of different format to enable it to meet the requirement of the screen for format and finally output the signal in the form of 24 bit RGB.

The standard of interface for PDP screen is LVDS (low voltage differential signal). So the digital RGB signal output from PW181 still needs to be converted into LVDS signal by the conversion interface chip of LVDS - N602 DS90C385 (This chip may vary with the manufacturer of the screen). This converted signal is in turn fed to the screen for driving purpose. The output of N602 is four pairs of differential signal and one pair of clock signal. If any pair of signal is abnormal then the image is affected to be abnormal for example, a certain color may become abnormal. The PWRDOWN signal output from PW181 is used to control the operation of N602, which works under low electric level.

PW181 is also the main CPU. Its program is stored in the externally connected flash N601. The software upgrading of RS-232 is actually the upgrading of the stored memory in N601 by PW181. The interface of menu is also produced by PW181. PW181 can automatically produce self check signal for trouble shooting.

3．3. Block diagram of PW181 is shown below:

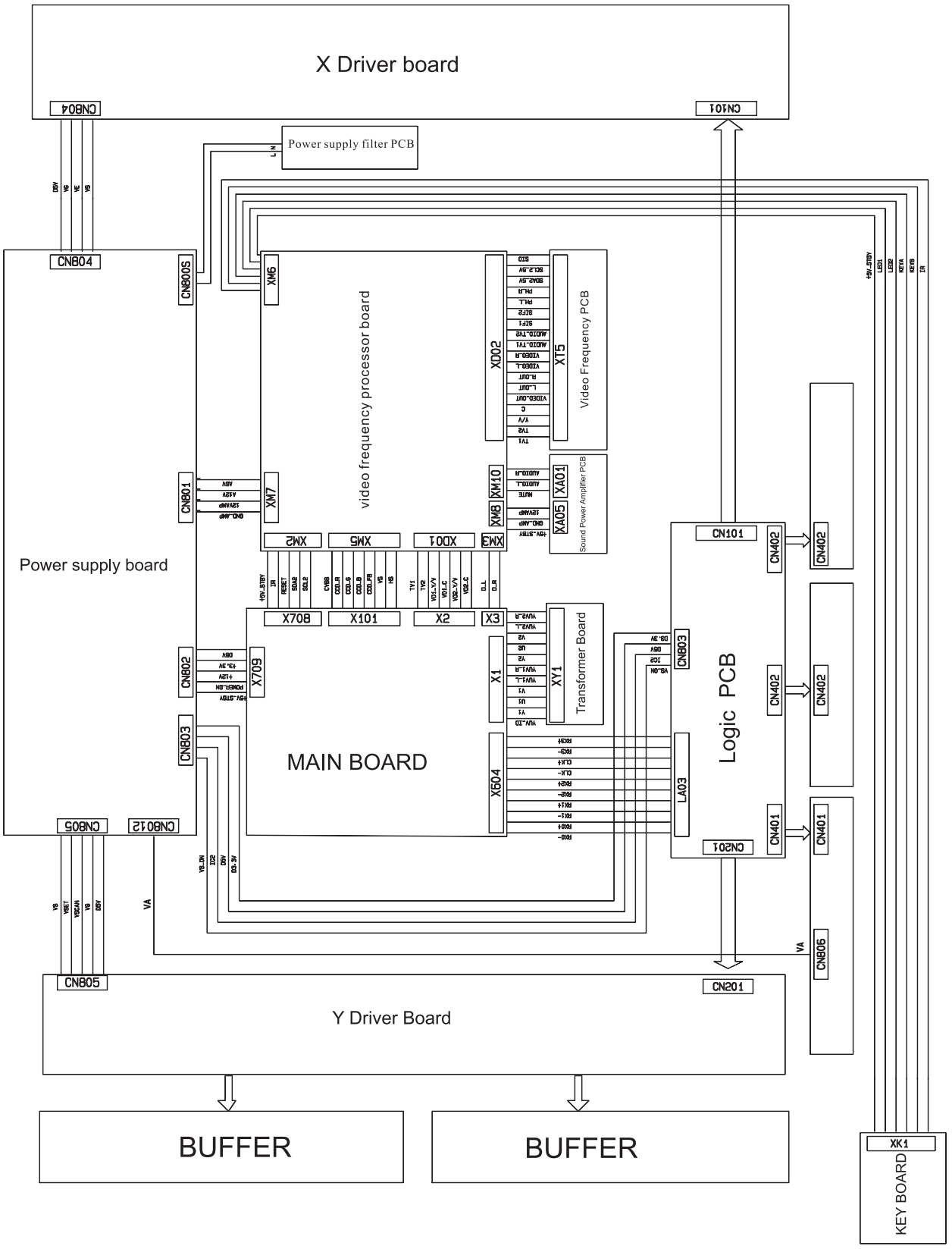


The above is a short account of the signal flow process of the TV series. Please note HS (Horizontal Synchronous), VS (Vertical Synchronous) and CLK (Clock), PEN (Enable) between individual stages are invariably the basic reference for the mode identification of lower level chip. Make sure that they are in normal working condition.

PW181 controls the standby of the complete TV set. The POWER-ON signal output from PORTB3 of PW181 is used to control the operation of the power supply board. When it is POWER_ON , the TV set is switched on with low electric level and is in standby with high electric level. When it's in standby the remaining power supply is only 5VSTBY.

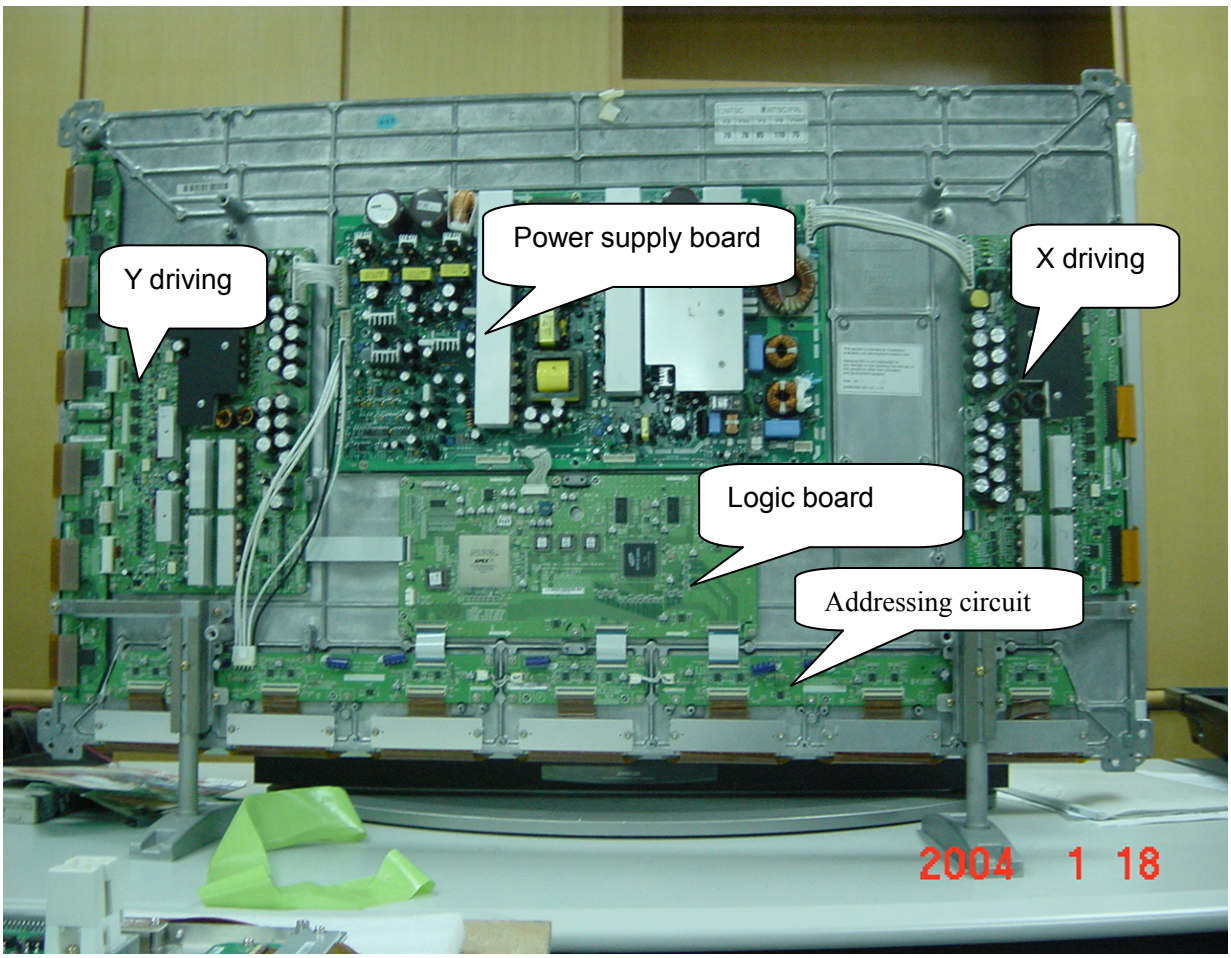
The voltage VS required by the operation of screen is also controlled by VS_ON output from logic board. It is in operation when the electric level is high. Only when the logic board receives correct signal (clock, synchronous, enable etc.) can VS_ON be correctly output. The operation of PDP screen has very high demand for the time sequence of power supply. If the time sequence is wrong it might make the screen unable to work normally.

Module connection diagram



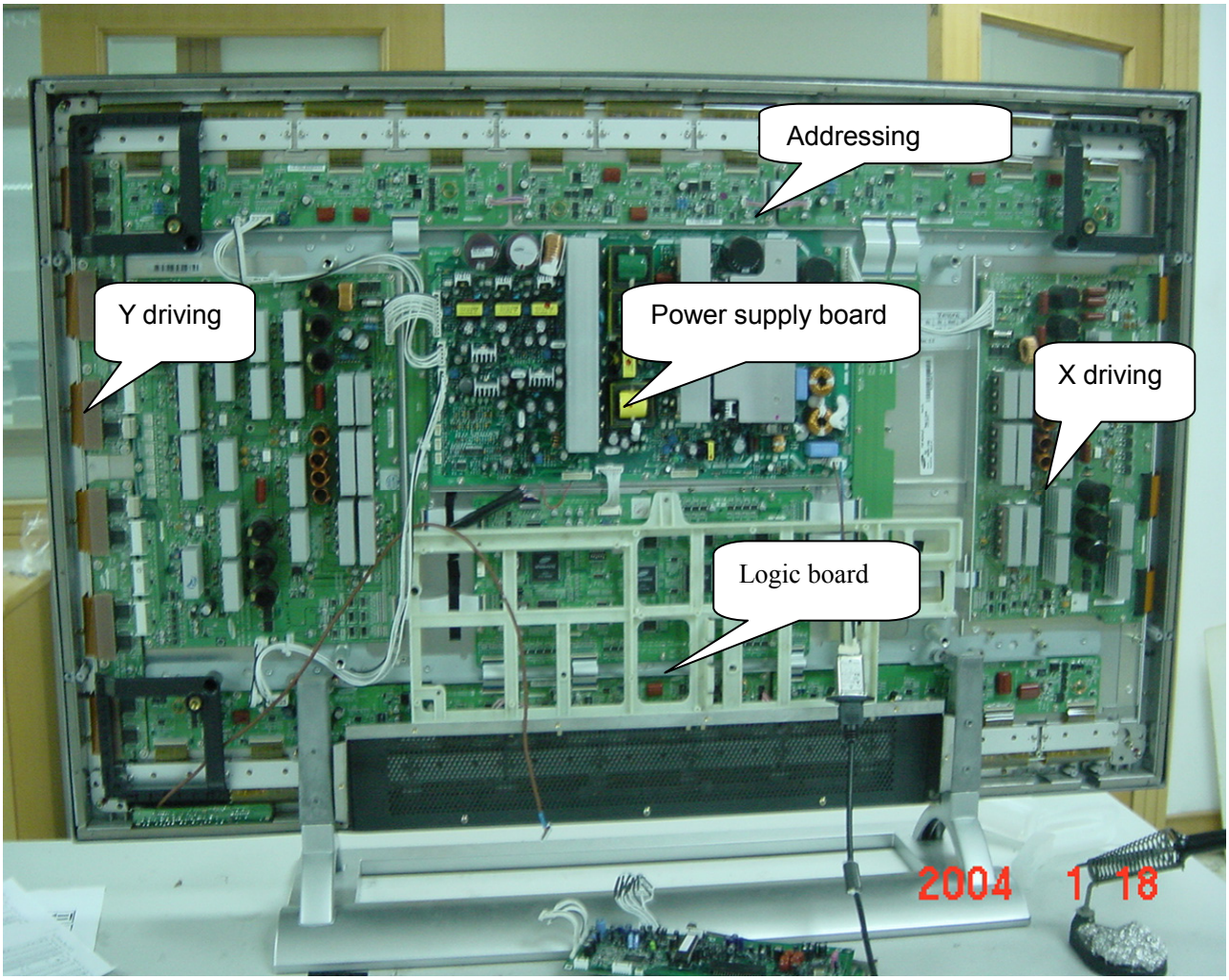
Distribution of the Circuit Board of Different Screens and their Functions

1、 42SD（Type:S42 SD-YD04，Code No:335-42001-00）



Parts designation	Function
Power supply board	Provide power for the operation of complete TV set
Logic board	Convert the LVDS signal from the processing board into the one displayable by screen
Addressing circuit	Addressing circuit for screen display, directly driving the address electrode on the screen (Vertical electrode, totally 852X3electrode）
X driving	X electrode（horizontal common holding electrode）driving circuit
Y driving	Y electrode（horizontal scanning, holding electrodes, total 480 electrode）driving circuit

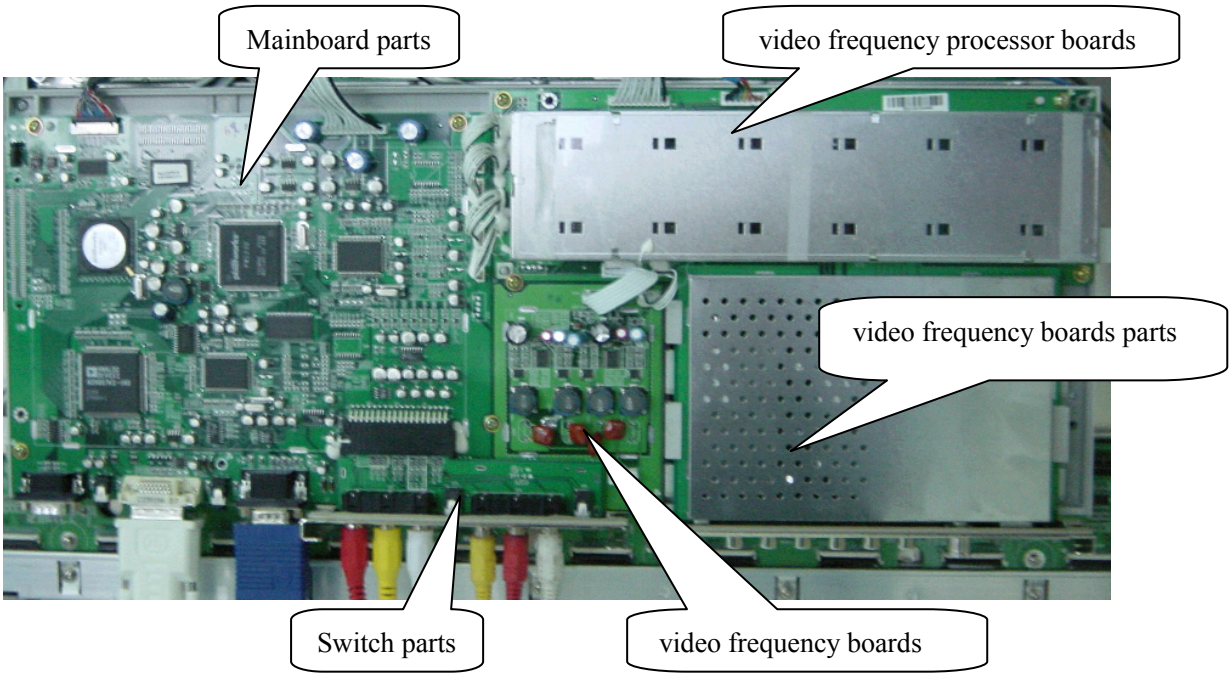
2、 50HD（Type:S50HW-XD02，Code No.:335-50001-00）



Parts designation	Function
Power supply board	Provide power for the operation of complete TV set
Logic board	Convert the LVDS signal from the processing board into the one displayable by screen
Addressing circuit	Addressing circuit for screen display, directly driving the address electrode on the screen (Vertical electrode, totally 1366X3electrodes) respectively driving for upper and lower half fields.
X driving	X electrode（horizontal common holding electrode）driving circuit
Y driving	Y electrode（horizontal scanning, holding electrodes, total 768 electrode）driving circuit

PCB parts and number

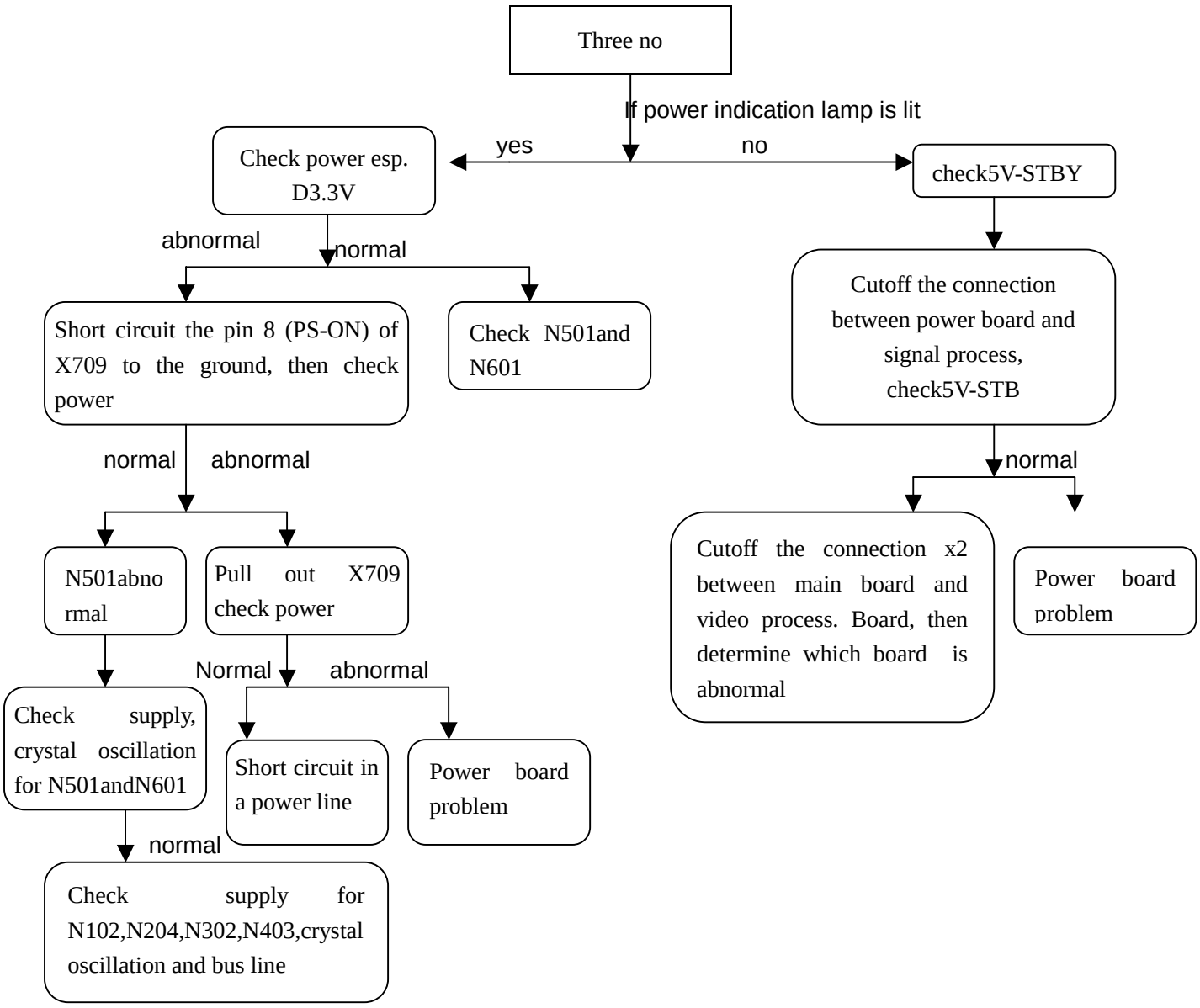
Singal processor boards:



Parts name	Parts number		Main parts and number
	PS-42D8	PH-50D8	
Main board	667-PHID8-01	667-PHSD8-01	N501 PW181-20 (353-01810-00) N204 PW1230 (353-12300-00) N403 AD9887-140 (353-98870-30) N102/N302 VPC3230D (353-32300-80) N602 DS90C385MTD (353-03850-20) N601 AM29LV800BT-90E(353-29800-10)
video frequency processor boards	667-PH42D8-40	667-PH50D8-40	NM5 SDA555XFL (352-05550-20) NM2 MSP3440G (353-34400-00) NM9 TDA7053AT (353-70530-70)
video frequency boards	667-PS42D8-70		TUNER1 JS-6B1/112A2-A2(590-40425-00) TUNER3 JS-6B1/111C6 (590-40422-00)
Sound amplification boards	667-PS42D8-24		NA01/NA02 TPA3001D (353-30010-10)
Transformer board	667-PS42D8-46		
Remote parts	301-UPS42D8-09		
key-press board parts	667-PH42D8-05	667-PH50D8-05	
power supply filter parTs	667-PH42D8-51	667-PH50D8-51	

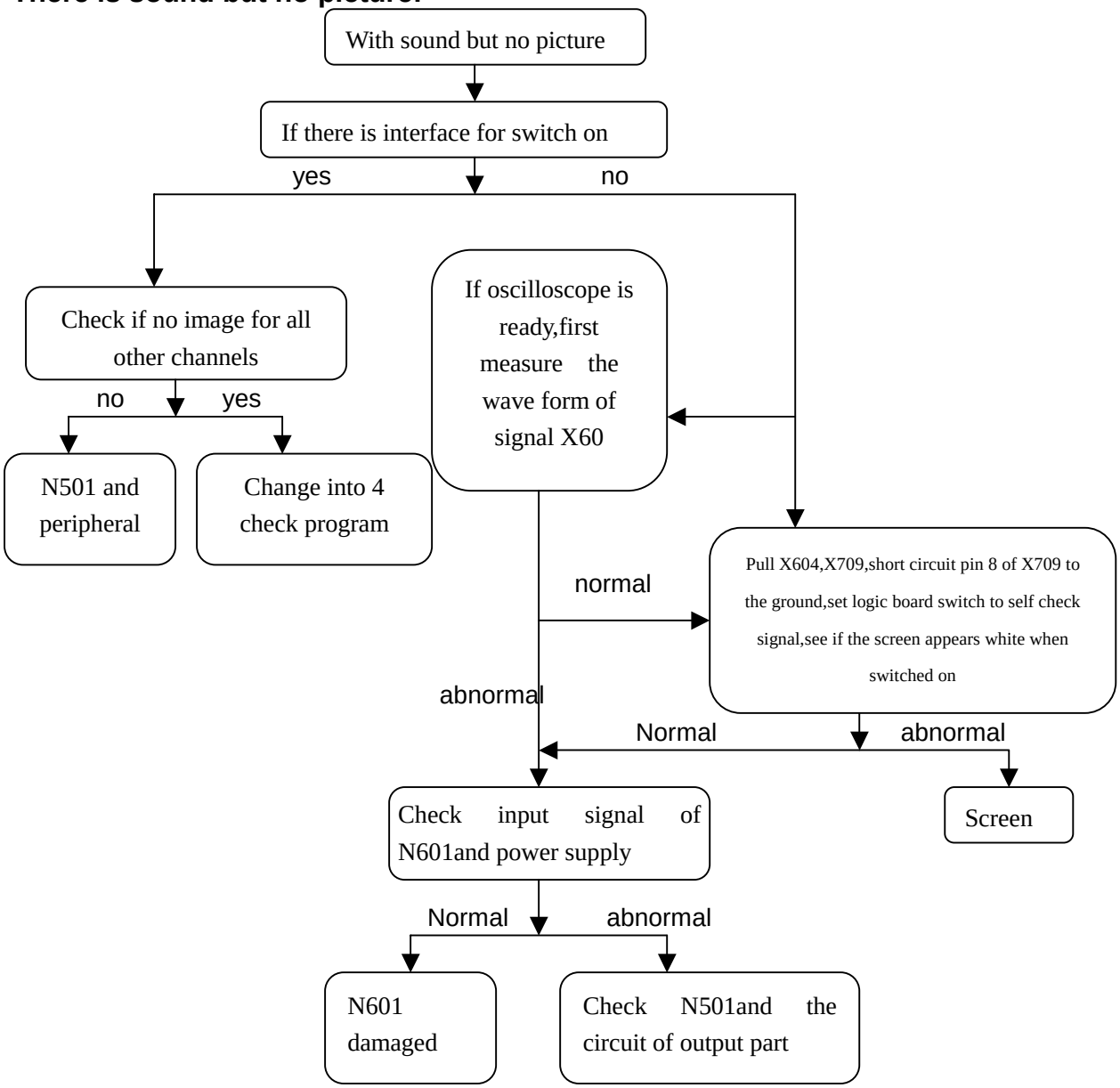
Diagram of Normal Trouble Shooting

1. “Three no”, i.e., no raster, no picture and not sound:


Three no
If power indication lamp is lit
yes
no
Check power esp. D3.3V
check5V-STBY
abnormal
normal
Short circuit the pin 8 (PS-ON) of X709 to the ground, then check power
Check N501and N601
Cutoff the connection between power board and signal process, check5V-STB
normal
normal
abnormal
N501abnormal
Pull out X709 check power
Cutoff the connection x2 between main board and video process. Board, then determine which board is abnormal
Power board problem
Normal
abnormal
Check supply, crystal oscillation for N501andN601
Short circuit in a power line
Power board problem
normal
Check supply for N102,N204,N302,N403,crystal oscillation and bus line

Note:Power supply for PDP is provided with over current and over voltage protection functions. If there is over current or over voltage, this protection will function and no output.

2． There is sound but no picture:


With sound but no picture
If there is interface for switch on
yes
no
Check if no image for all other channels
no
yes
N501 and peripheral
Change into 4 check program
If oscilloscope is ready,first measure the wave form of signal X60
normal
Pull X604,X709,short circuit pin 8 of X709 to the ground,set logic board switch to self check signal,see if the screen appears white when switched on
abnormal
Normal
abnormal
Screen
Check input signal of N601and power supply
Normal
abnormal
N601 damaged
Check N501and the circuit of output part

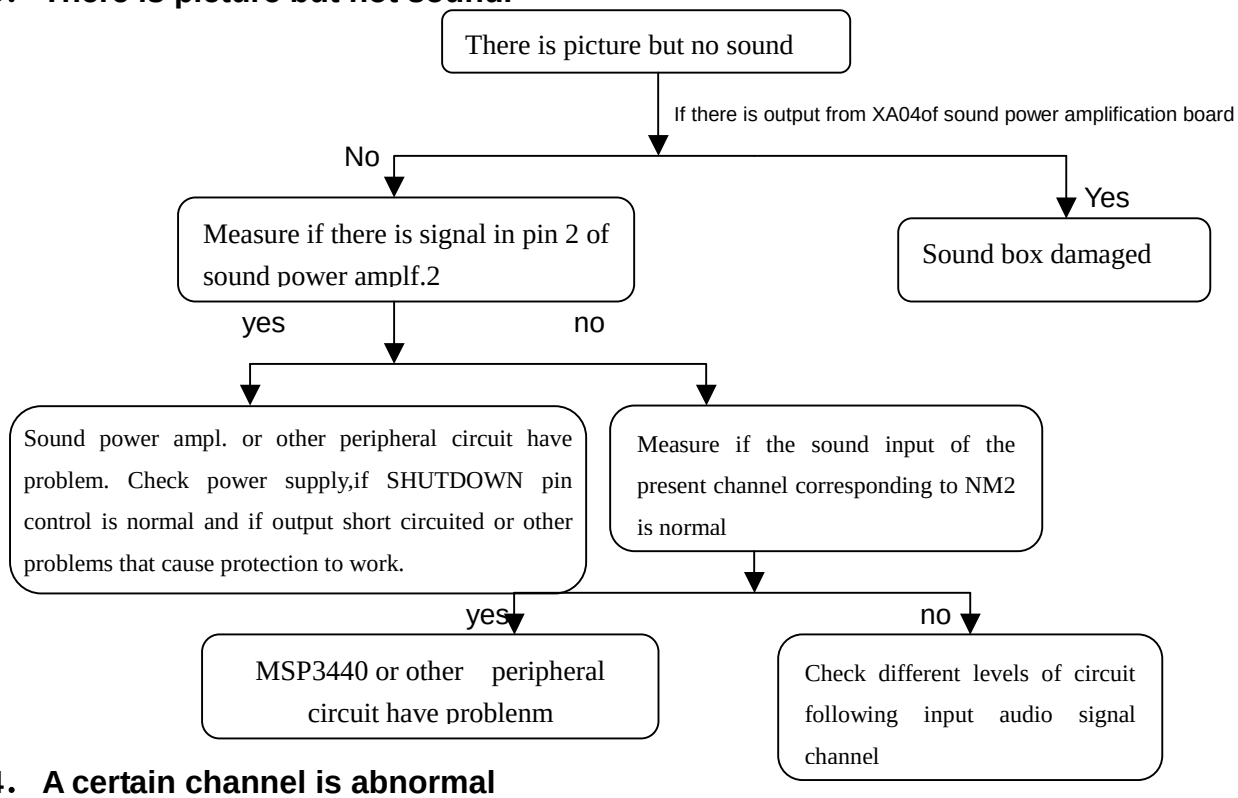
Note:

- For the originally self-powered software, if the operation of PW181 is abnormal, in SDA555X there may be a state of individually switched-on. In this case very often the phenomenon of the trouble is there is sound but no image.
- Setting up for the self check of the screen:

  - For 42”SD screen (S42SD-YD04):Push down 2 and 4 and push up 3 of SW2001on the logic board;
  - For 50”HD screen (S50HW-XD02):Push down 1 and 4 and push up 2, 3, 5, 6 of SW2001on the logic board;

  Please make sure resume it to the original status when the check is over.

3. There is picture but not sound.

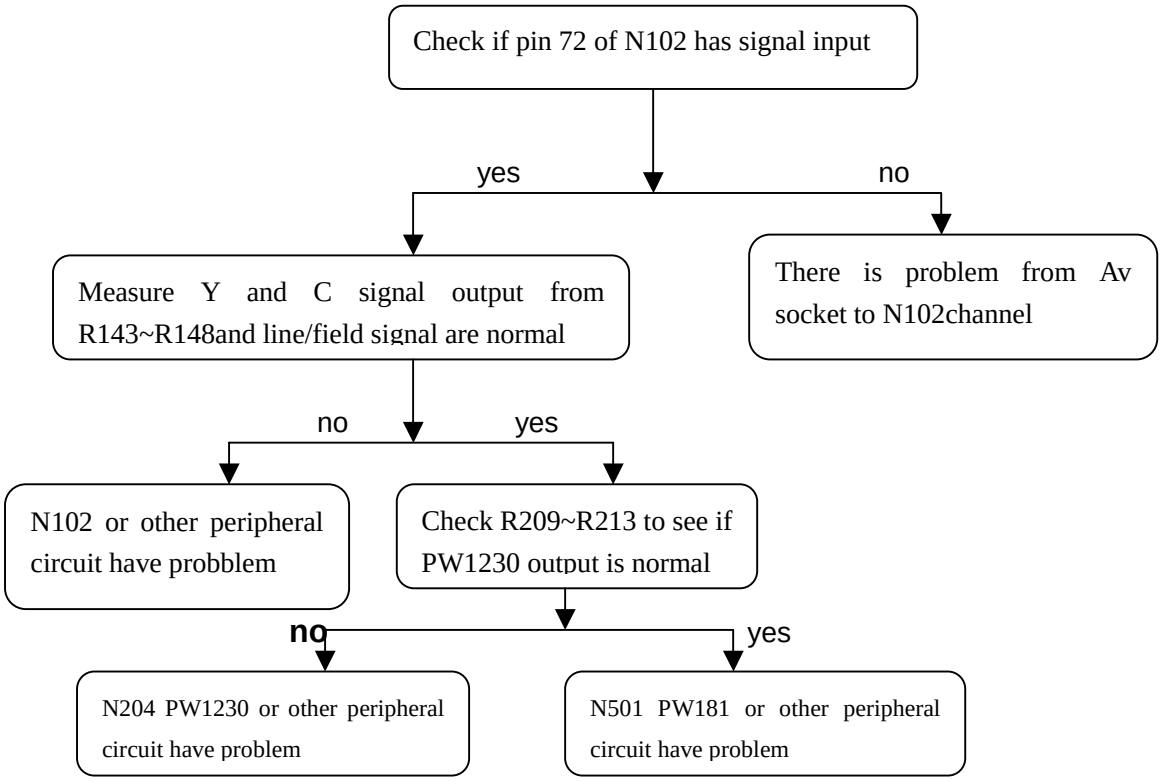

There is picture but no sound
If there is output from XA04of sound power amplification board
No
Yes
Measure if there is signal in pin 2 of sound power amplf.2
Sound box damaged
yes
no
Sound power ampl. or other peripheral circuit have problem. Check power supply,if SHUTDOWN pin control is normal and if output short circuited or other problems that cause protection to work.
Measure if the sound input of the present channel corresponding to NM2 is normal
yes
no
MSP3440 or other peripheral circuit have problenm
Check different levels of circuit following input audio signal channel

4. A certain channel is abnormal

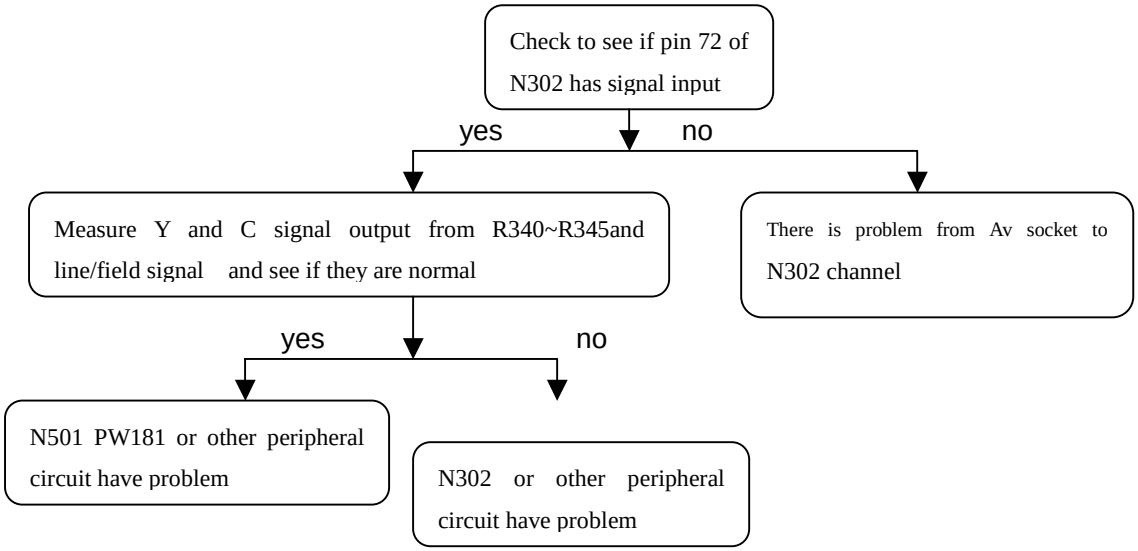
1) AV no picture

First, use dual picture function to judge if the main or sub picture has problem.

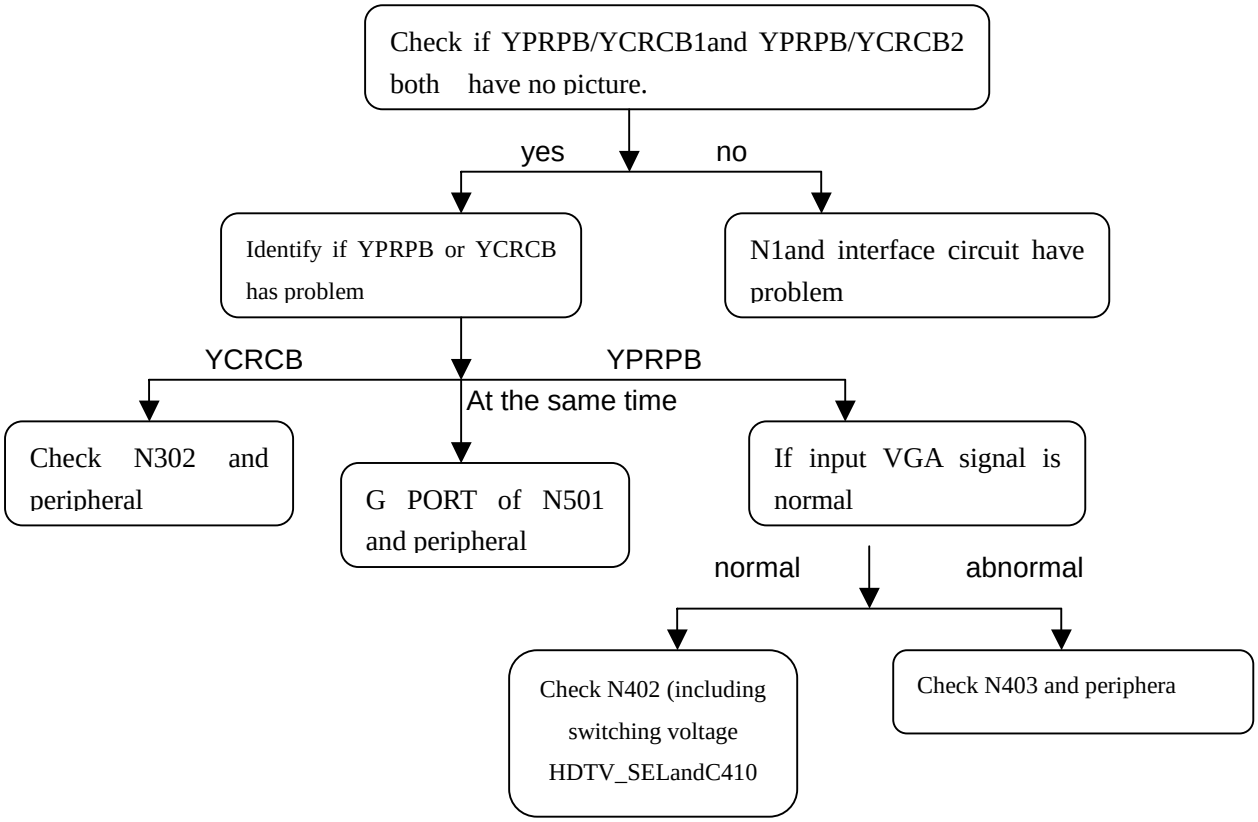
No picture in main channel:


Check if pin 72 of N102 has signal input
yes
no
Measure Y and C signal output from R143~R148and line/field signal are normal
There is problem from Av socket to N102channel
no
yes
N102 or other peripheral circuit have probblem
Check R209~R213 to see if PW1230 output is normal
no
yes
N204 PW1230 or other peripheral circuit have problem
N501 PW181 or other peripheral circuit have problem

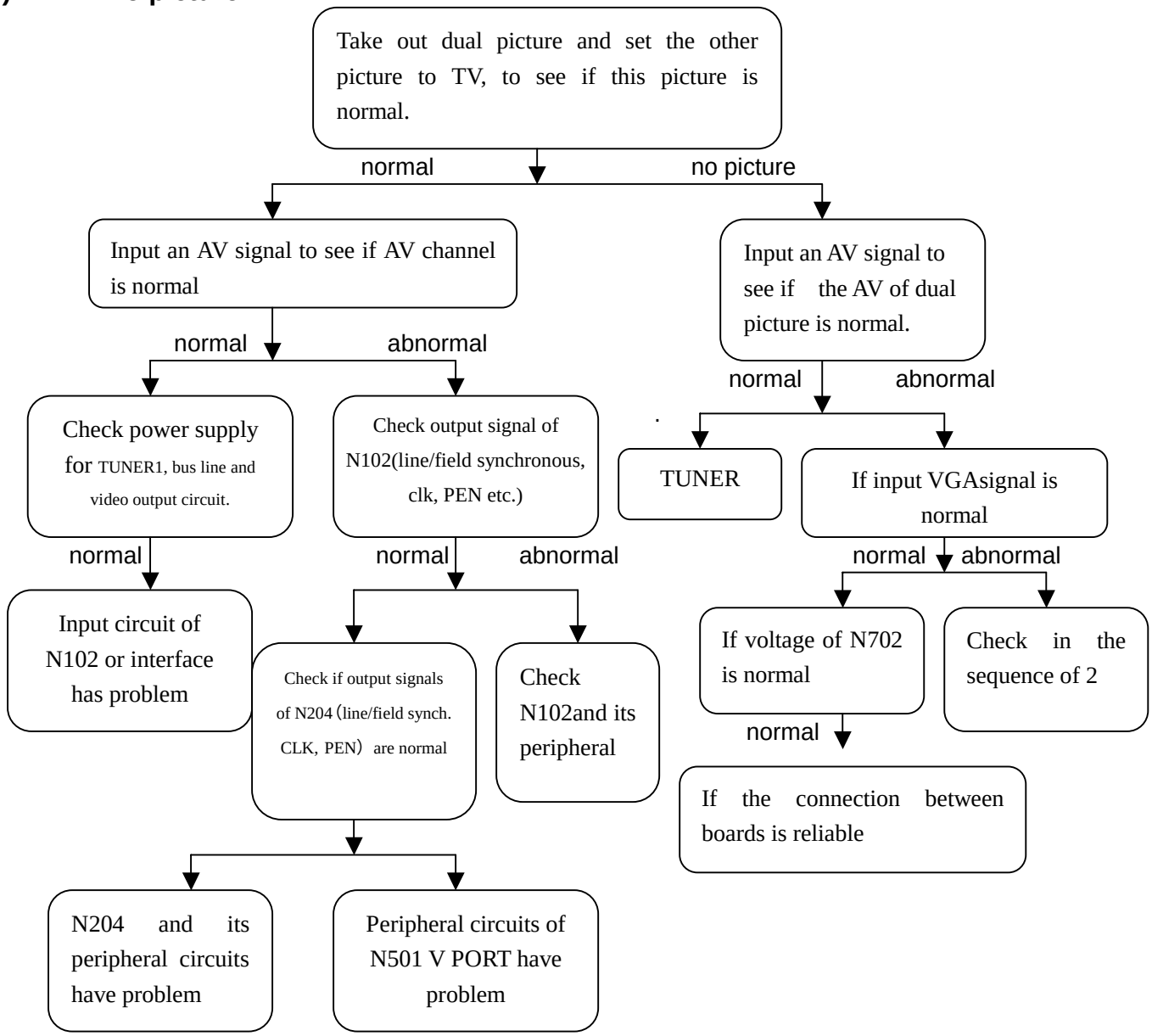
No picture in sub channel:


Check to see if pin 72 of N302 has signal input
yes
no
Measure Y and C signal output from R340~R345and line/field signal and see if they are normal
There is problem from Av socket to N302 channel
yes
no
N501 PW181 or other peripheral circuit have problem
N302 or other peripheral circuit have problem

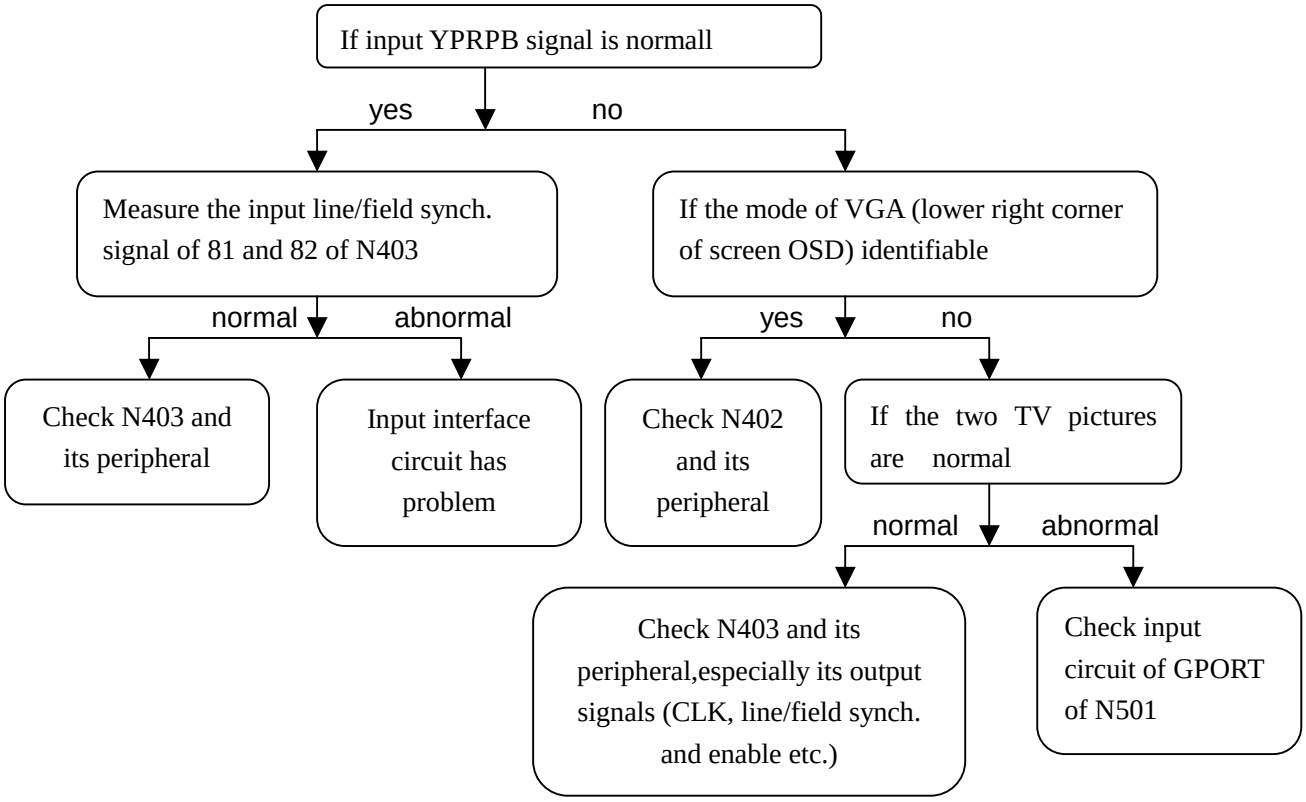
3) No picture in YPRPB or YCRCB



4) TV no picture


Take out dual picture and set the other picture to TV, to see if this picture is normal.
normal
no picture
Input an AV signal to see if AV channel is normal
normal
abnormal
Check power supply for TUNER1, bus line and video output circuit.
normal
Input circuit of N102 or interface has problem
Check output signal of N102(line/field synchronous, clk, PEN etc.)
normal
abnormal
Check if output signals of N204（line/field synch. CLK, PEN） are normal
Check N102and its peripheral
N204 and its peripheral circuits have problem
Peripheral circuits of N501 V PORT have problem
Input an AV signal to see if the AV of dual picture is normal.
normal
abnormal
TUNER
If input VGAsignal is normal
normal
abnormal
If voltage of N702 is normal
Check in the sequence of 2
normal
If the connection between boards is reliable

4) VGA No Picture


If input YPRPB signal is normall
yes
no
Measure the input line/field synch. signal of 81 and 82 of N403
If the mode of VGA (lower right corner of screen OSD) identifiable
normal
abnormal
yes
no
Check N403 and its peripheral
Input interface circuit has problem
Check N402 and its peripheral
If the two TV pictures are normal
normal
abnormal
Check N403 and its peripheral,especially its output signals (CLK, line/field synch. and enable etc.)
Check input circuit of GPORT of N501

6) DVI no picture

If VGA works normally, it's enough only to check the connection between socket X401and N403 and the operation status of N403. R414 is the matching resistance for its input. If it has problem the DVI image would become abnormal.

5. Abnormal picture :

- Peculiar color, which may be caused by the following phenomena:

  - A certain differential wire pair of LVDS（RX0+/-，RX1+/-，RX2+/-，RX3+/-） is abnormal, which may lead to lack of color (it's not a complete loss of color);
  - Failure with resistor rows R550~R555，which may lead to loss of corresponding color from the gray degree corresponding to the picture of all channels. Through self signal check by PW181, the failure is still there.
  - Failure with resistor rows R419, R421, R425, R427, R431, R432，which may lead to loss of corresponding color from the gray degree corresponding to the picture of channels VGA/YPRPB/DVI.
  - Failure with resistor rows R415, R418, R422, R424, R429, R430，which may lead to loss of corresponding color from the gray degree corresponding to the picture of channel DVI.
  - Failure with resistor rows R342, R343, R344, R345，which may lead to loss of corresponding color from the gray degree corresponding to the picture of sub-channels TV/AV/YCRCB, or lead to abnormal brightness.

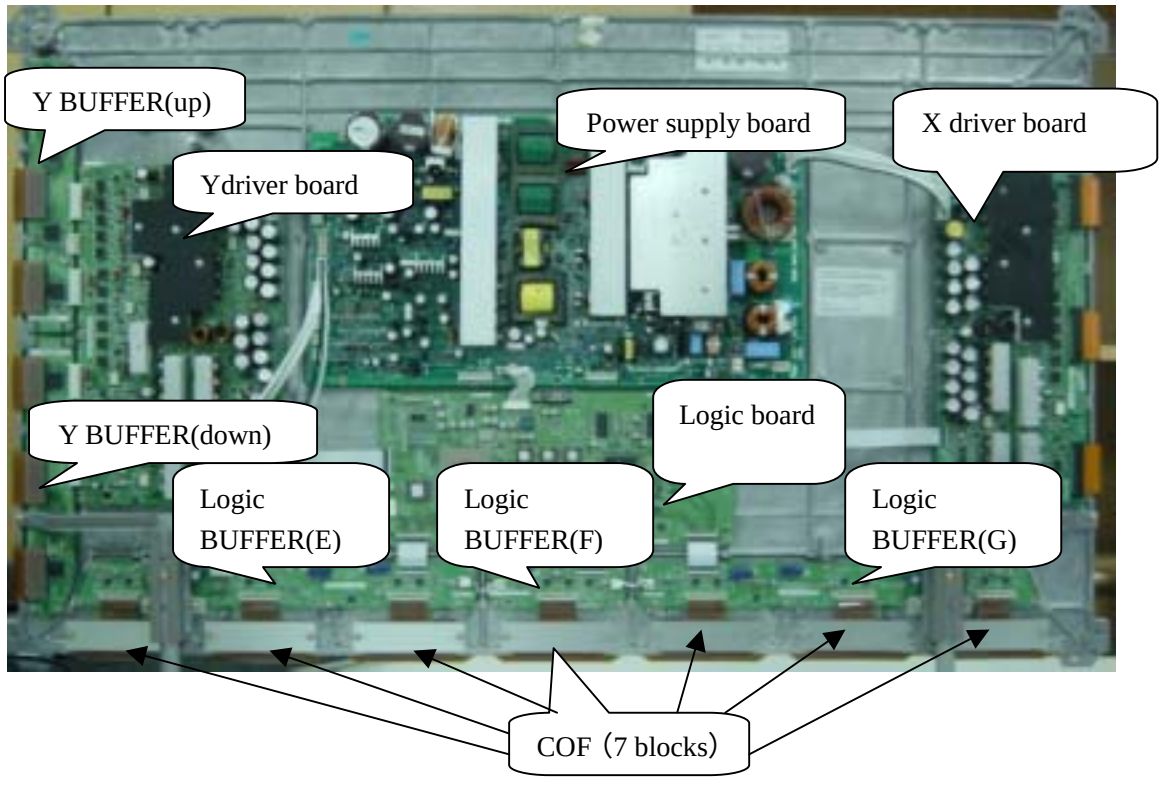
- Failure with resistor rows R207, R208, R209, R210, R211, R212 or R145, R146, R147, R148，which may lead to loss of corresponding color from the gray degree corresponding to the picture of main channels TV/AV, or lead to abnormal brightness.
- Bad connection between N203 and N204, which may also lead to abnormal picture (column bar like) in main channel TV/AV.

- Abnormal picture vertically or horizontally (bar like): Abnormal in complete line extending all the way from up downward on the screen of stand definition TV setr; abnormal vertically on half screen of high definition TV set. They may be caused by the damage of the address BUFFER module that directly corresponds to its position, or may be caused by the damage of the connection wire that directly corresponds to the position of the screen. The horizontal bar like abnormality is also related to the Y driving circuit that corresponds directly to its position. To judge these phenomena, It's possible to check it by setting the screen to the status of self check as explained above
- No brightness in the square block area: Normally it's caused by the damage of the address BUFFER module that directly corresponds to its position, or may be caused by the damage of the connection wire that directly corresponds to the position of the screen. To judge these phenomena, It's possible to check it by setting the screen to the state of self check as explained above

Diagnosis for Plasma Screen of PS42D8

And Maintenance of the Functions of Various Modules on Screen

As shown in the figure below, PDP screen can be divided into power supply board, X driving board, Y driving board, logic board, logic BUFFER board (E, F, G), Y BUFFER board (upper and lower), COF etc.:



*** Power supply board**: to supply power for the screen, other functional modules on the screen, our own main board, and video frequency processing board.

*** X driving board**: to produce and provide driving signal for X electrode according to the time sequence signal sent from logic board.

*** Y driving board**: to produce and provide driving signal for Y electrode according to the time sequence signal sent from logic board.

***Logic board:** to process the image signal sent from the main board, to produce addressing signal and to provide driving signal for X and Y driving boards.

***Logic BUFFER board (E, F):** To convert the data signal and control signal sent from the logic board into the signals required by COF

***Y BUFFER board（Upper，Lower）:** to transmit the scanning signal from the Y driving board to the screen, which is divided into upper and lower parts.

***COF:**to convert the signal sent from the logic BUFFER board into the address signal used by the screen.

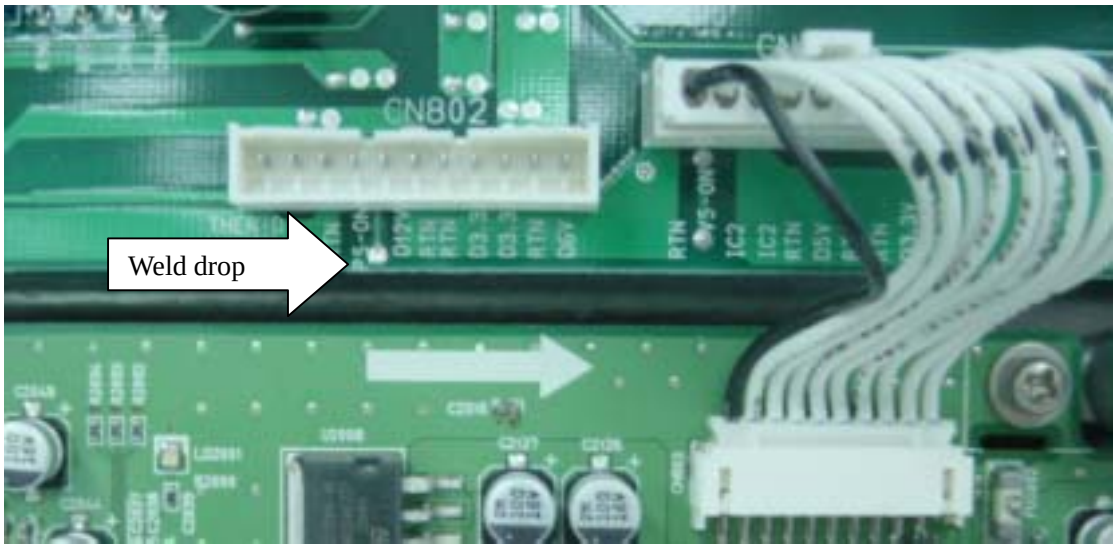
II. Trouble diagnosis:

1. The screen is not bright:

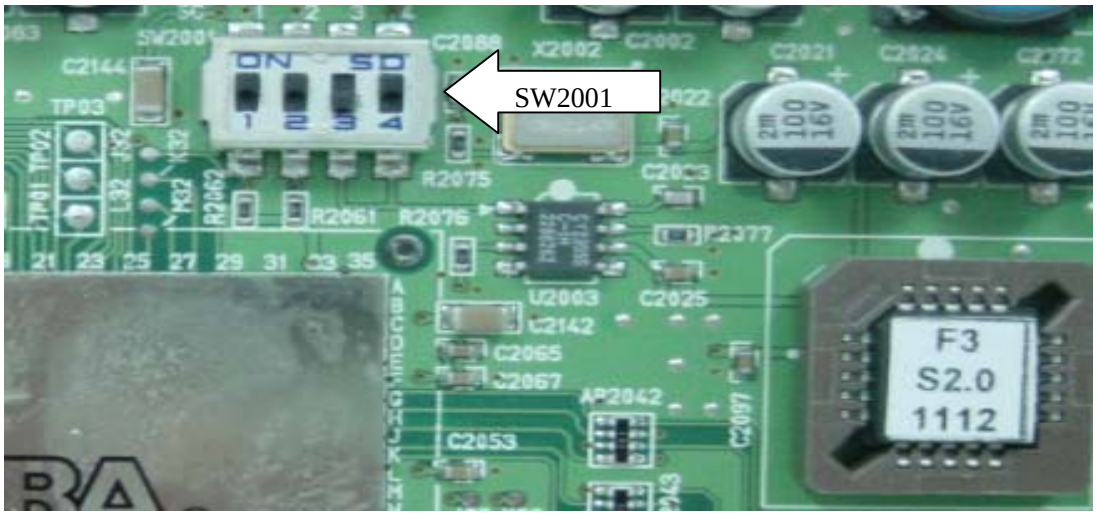
a. Check to see if the power supply plug from the power filter board to the power supply board is well inserted into the socket. If not, plug it in.

b. Check if the fuse on the power supply board is blown up. If yes, replace it for a good one.

c. Remove our main board and the video frequency processing board, ground the pin 4 POWER_ON/OFF of socket CN802 of the power supply board,



and then push the slide switch SW2001 on the logic board to the internal modes (1, 3 up and 2, 4 down) from external modes (1, 2, 4 up and 3down)

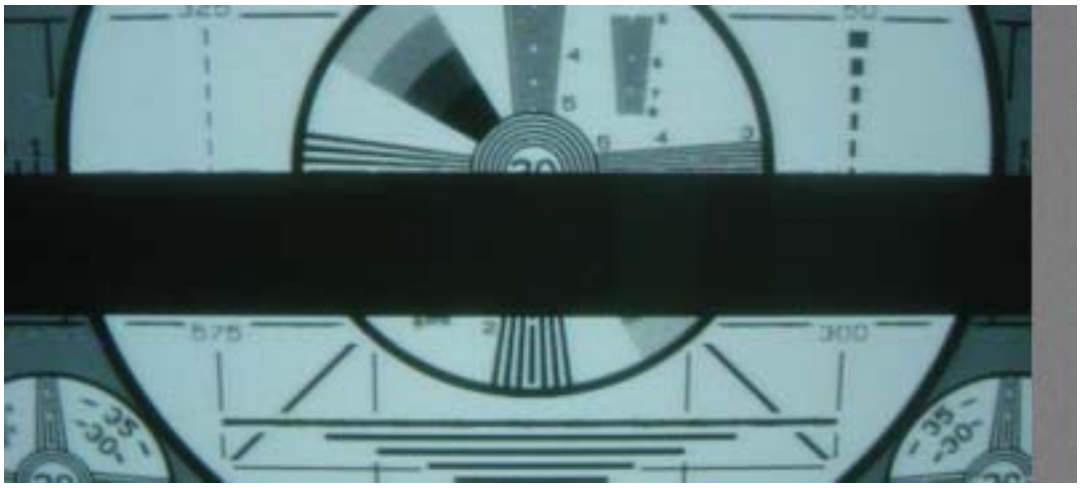


Switch the power on and see if the screen is lit. If the screen can give a normal and completely white field signal, then the problem lies in our main board or video frequency processing board, which will be dealt with separately.

d. If the screen is not lit, then first replace the power supply board to see if the problem is solved.

e. If the problem remains after the power supply board is replaced, then the problem lies in the screen. Replace the entire screen for treatment.

2. There appears on the screen a line or several unlit lines.

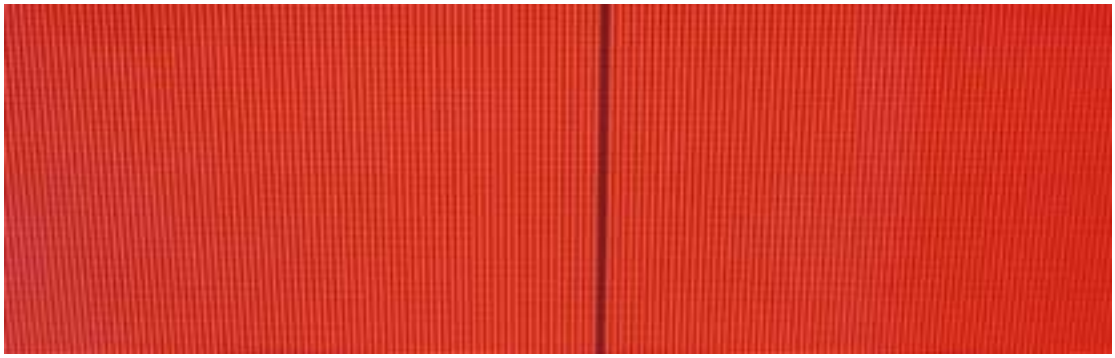


Check if the socket between Y driving board and Y BUFFER is plugged well. If not, plug it well. If yes then replace Y BUFFER (upper, lower) in respect to the upper , lower part of the dark line on the screen.

3. There appear on the screen one or several horizontal lines that are much brighter than the remaining horizontal lines at the edge:

   Check if the socket between Y driving board and Y BUFFER is plugged well. If not, plug it well. If yes then replace Y BUFFER (upper, lower) in respect to the upper , lower part of the dark line on the screen.

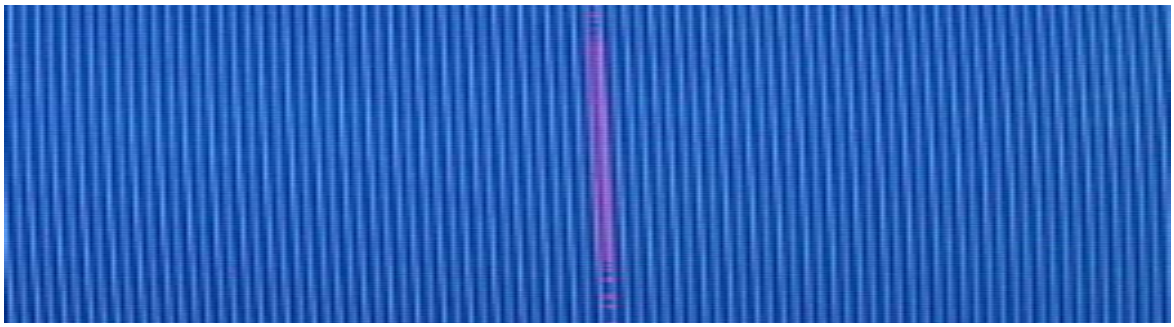
4. There appear on the screen one vertical unlit line or a vertical entirely unlit block



a. If it's one vertical unlit line, then COF has problem.

b. If it's a vertical entirely unlit block, then first check if the connection socket between COF and logic BUFFER has problem. If not, check if the connection socket between the logic BUFFER and the logic board is normal. If yes, replace the logic BUFFER. Finally, if the problem still remains when the replacement is over, then replace the logic board.

5. There appears on the screen a mono color signal and one or several vertical bright lines of other colors:



a. If it's a vertical bright line of other colors, then the problem lies with COF or the screen.

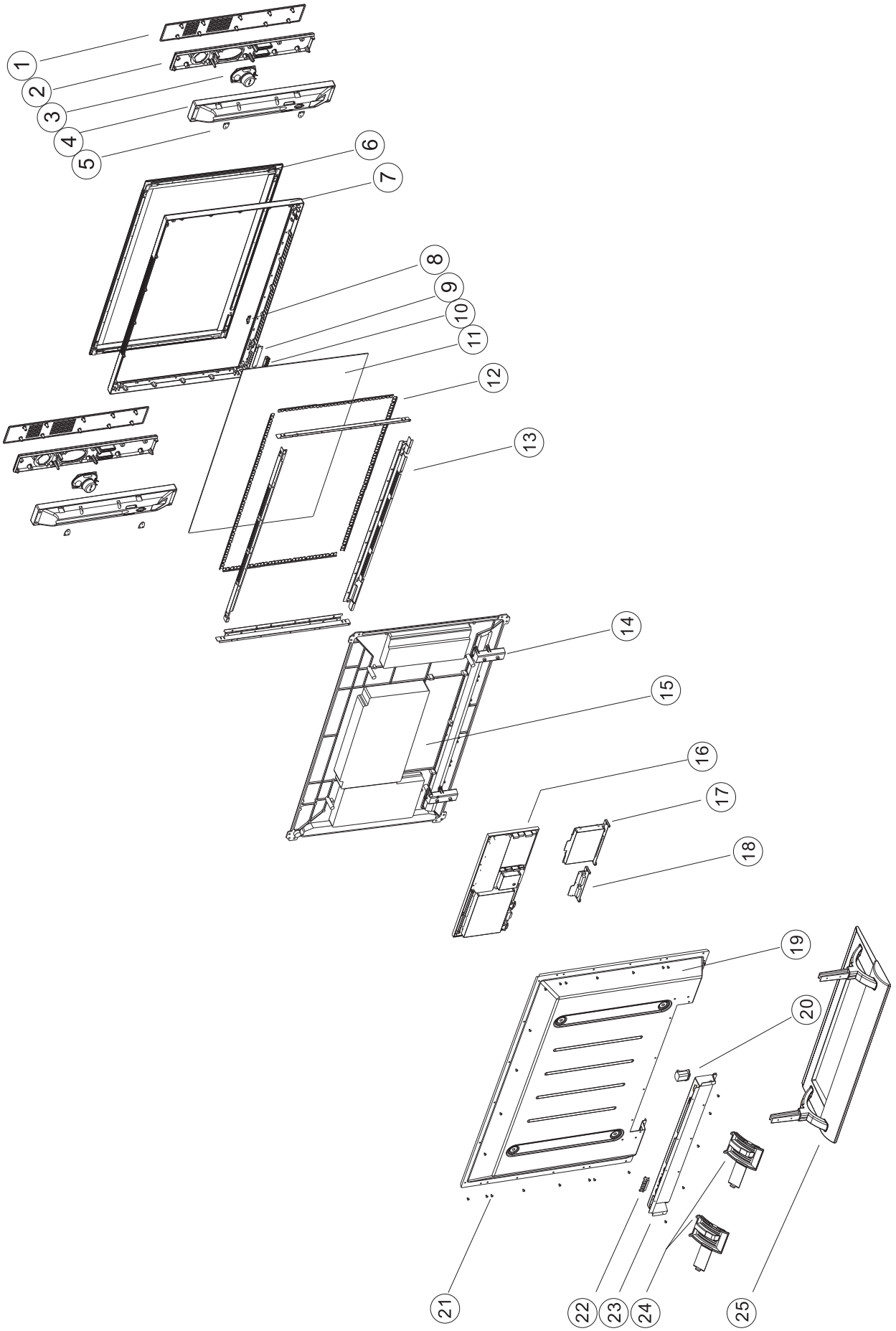
b. If it's an entire vertical block of other colors, then first check to see if the connection socket between COF and logice BUFFER has problem. If no problem, check if the connection socket between the logic BUFFER and the logic board is normal. If it's normal, then replace the logic BUFFER. If the problem still remains after the replacement, then replace the logic board. Finally if the problem is still there, then the problem lies with COF.

6. There appear on the screen abnormal bright spots or blocks that are different from what's described above:

a. Check if the connection socket between COF and logic BUFFER board has been well plugged.

b. Replace the logic BUFFER board. If it's not solved then replace logic board. If the problem still remains, then it's the problem with COF.

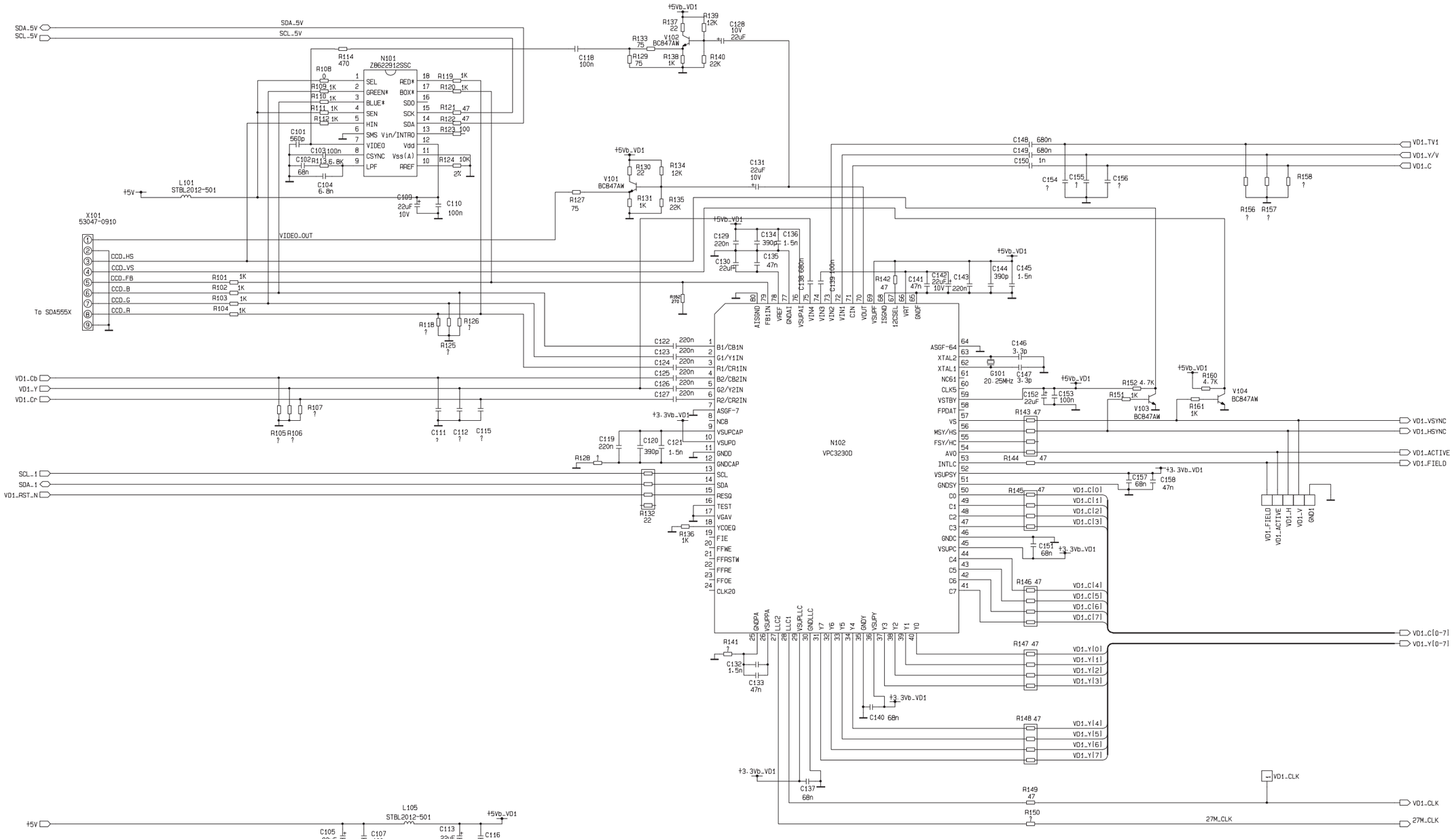
INSTALLATION DRAWING

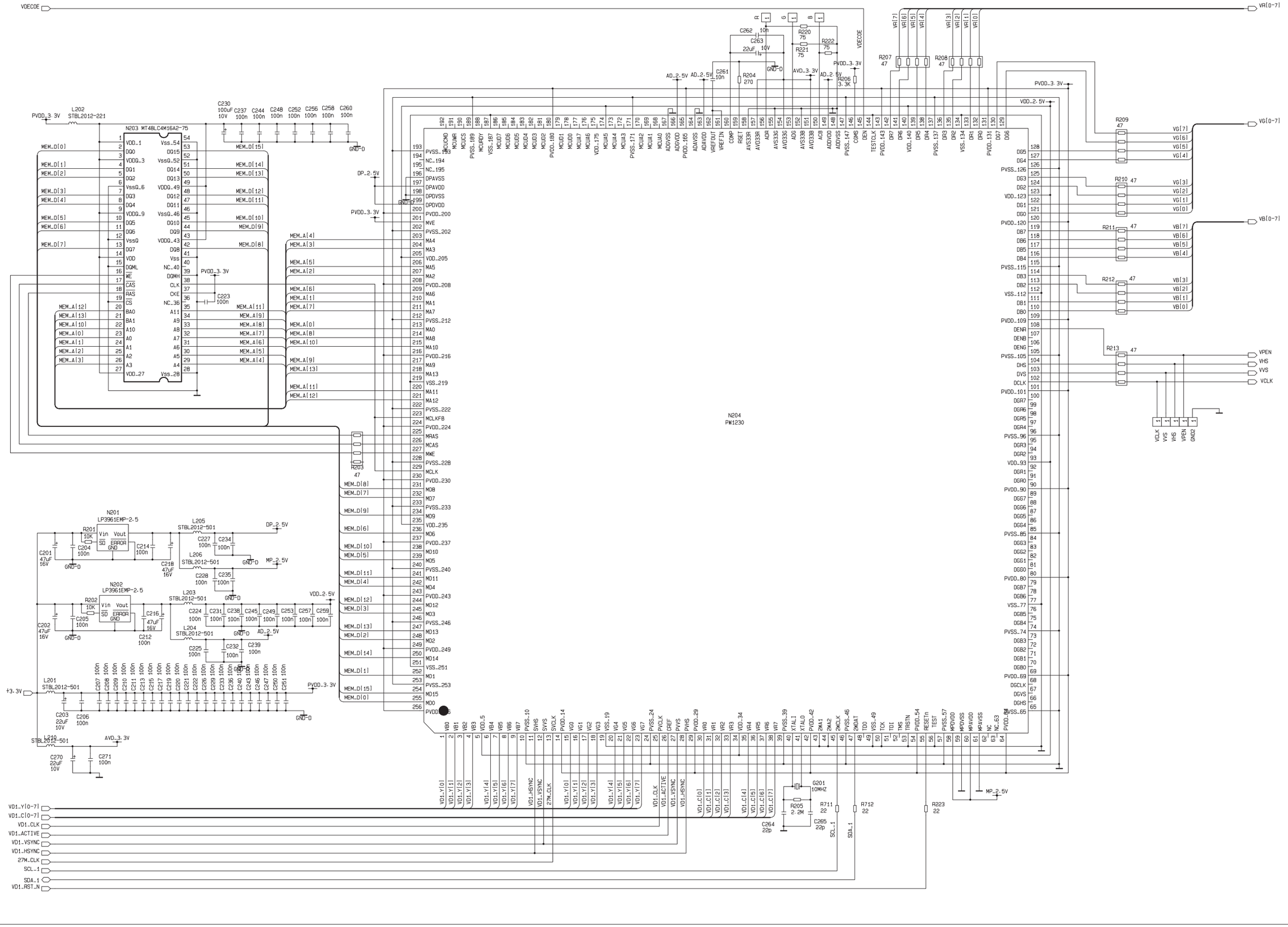


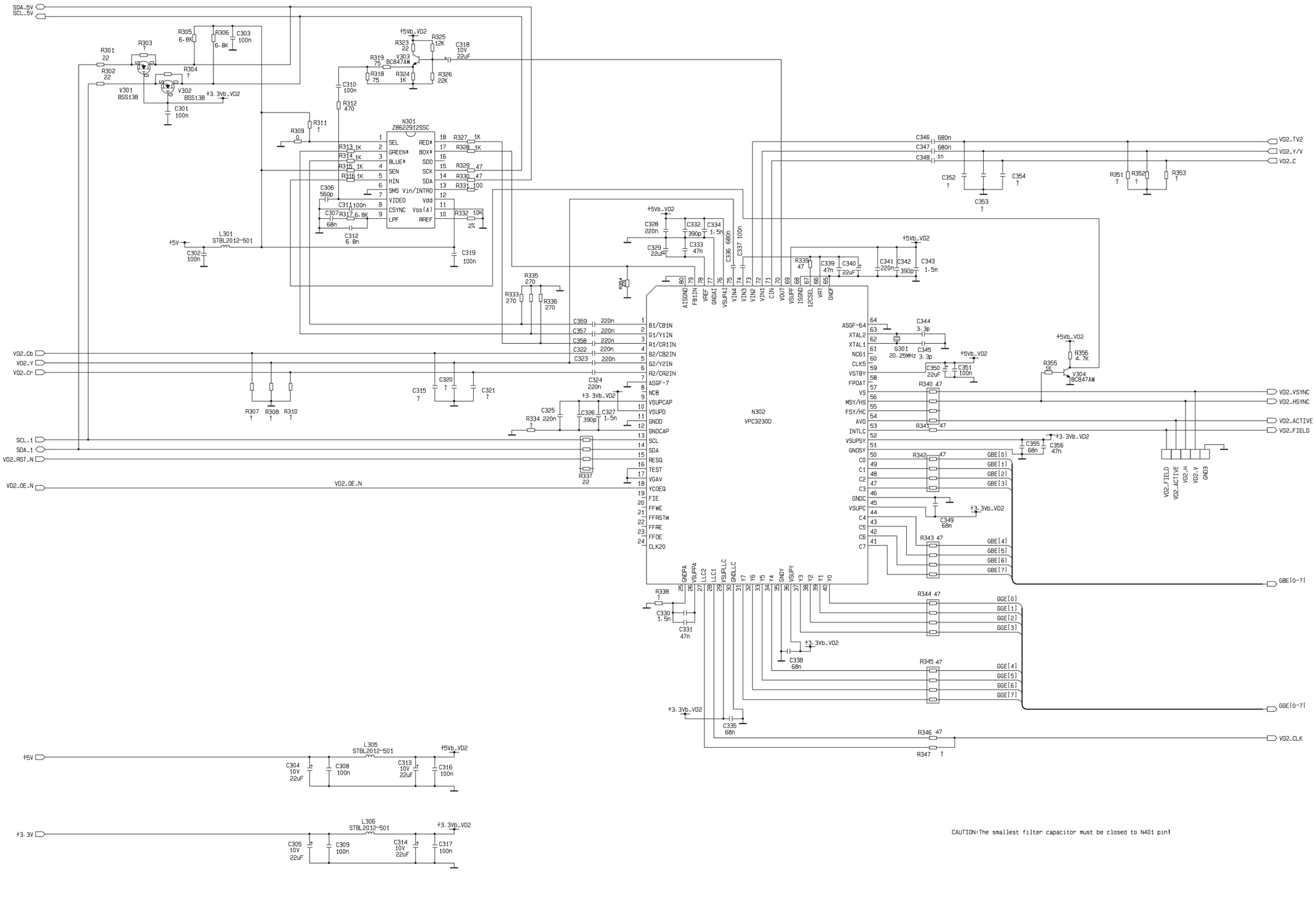
SCHEMATIC DIAGRAM

MAIN BOARD

Interface(PS-420B)
2003/09/30
Version1.3
XOCECO


SDA_5V
SCL_5V
N101
ZR62912SSC
SEL
GREEN*
BLUE*
SEN
HIN
SMS
VIDEO
CSYNC
LPF
RED*
BOX*
SDO
SCK
SDA
Vin/INTRO
Vdd
Vss(A)
AREF
+5Vb_VD1
V102 BC847AW
V101 BC847AW
L101 STBL2012-501
+5V
X101 53047-0910
VIDEO_OUT
CCD_HS
CCD_VS
CCD_FB
CCD_B
CCD_G
CCD_R
To SDA555X
VD1_Cb
VD1_Y
VD1_Cr
SCL_1
SDA_1
VD1_RST_N
N102
VPC3230D
B1/CB1N
G1/Y1N
R1/CR1IN
B2/CB2IN
G2/Y2IN
R2/CR2IN
ASGF-7
NCB
VSUPCAP
VSUPD
GNDD
GNDCAP
SCL
SDA
RESQ
TEST
VGAV
YCOEQ
FIE
FFWE
FFRSTW
FFRE
FFOE
CLK20
ASGF-64
XTAL2
XTAL1
NC61
CLK5
VSTBY
FPDAT
VS
MSY/HS
FSY/HC
AVO
INTLC
VSUPSY
GNDSY
C0
C1
C2
C3
GNDC
VSUPC
C4
C5
C6
C7
VD1_C[0]
VD1_C[1]
VD1_C[2]
VD1_C[3]
VD1_C[4]
VD1_C[5]
VD1_C[6]
VD1_C[7]
VD1_C[0-7]
VD1_Y[0]
VD1_Y[1]
VD1_Y[2]
VD1_Y[3]
VD1_Y[4]
VD1_Y[5]
VD1_Y[6]
VD1_Y[7]
VD1_Y[0-7]
VD1_TV1
VD1_Y/V
VD1_C
VD1_VSYNC
VD1_HSYNC
VD1_ACTIVE
VD1_FIELD
VD1_CLK
27M_CLK
GND
L105 STBL2012-501
L106 STBL2012-501
+3.3V
+3.3Vb_VD1
CAUTION:The smallest filter capacitor must be closed to N201 pin!


VDECOE
N203 MT48LC4M16A2-75
N204
PW1230
N201
LP3961EMP-2.5
N202
LP3961EMP-2.5
L202
STBL2012-221
L201
STBL2012-501
L203
STBL2012-501
L204
STBL2012-501
L205
STBL2012-501
L206
STBL2012-501
L210
STBL2012-501
PVDD_3.3V
VDD_2.5V
AVD_3.3V
AD_2.5V
DP_2.5V
MP_2.5V
GND-D
+3.3V
VA[0-7]
VB[0-7]
VG[0-7]
VPEN
VHS
VVS
VCLK
VD1_Y[0-7]
VD1_C[0-7]
VD1_CLK
VD1_ACTIVE
VD1_VSYNC
VD1_HSYNC
27M_CLK
SCL_1
SDA_1
VD1_RST_N
G201
10MHZ


SDA_5V
SCL_5V
R301 22
R302 22
R303 ?
R304 ?
R305 6.8K
R306 6.8K
C303 100n
V301 BSS138
V302 BSS138
+3.3Vb_VD2
C301 100n
+5Vb_VD2
R323 22
R325 12K
C318 10V 22uF
V303 BC847AW
R319 75
R318 75
R324 1K
R326 22K
C310 100n
R312 470
R309 0
R311 ?
N301 Z8622912SSC
SEL
GREEN*
BLUE*
SEN
HIN
SMS Vin/INTRO
VIDEO
CSYNC
LPF
RED*
BOX*
SDO
SCK
SDA
Vdd
Vss(A)
AREF
R313 1K
R314 1K
R315 1K
R316 1K
R317 6.8K
R327 1K
R328 1K
R329 47
R330 47
R331 100
R332 10K
2K
C306 560p
C311 100n
C307 68n
C312 6.8n
+5V
L301 STBL2012-501
C302 100n
C319 100n
R335 270
R333 270
R336 270
R334 ?
C325 220n
C326 390p
C327 1.5n
C328 220n
C329 22uF
C332 390p
C334 1.5n
C333 47n
C335 680n
C337 100n
R339 47
C339 47n
C340 22uF
C341 220n
C342 390p
C343 1.5n
C346 680n
C347 680n
C348 1n
C352 ?
C353 ?
C354 ?
R351 ?
R352 ?
R353 ?
VD2_TV2
VD2_Y/V
VD2_C
VD2_Cb
VD2_Y
VD2_Cr
R307 ?
R308 ?
R310 ?
C315 ?
C320 ?
C321 ?
C322 220n
C323 220n
C324 220n
C357 220n
C358 220n
C359 220n
B1/CB1IN
G1/Y1IN
R1/CR1IN
B2/CB2IN
G2/Y2IN
R2/CR2IN
ASGF-7
NCB
VSUPCAP
VSUPD
GNDD
GNDCAP
SCL
SDA
RESQ
TEST
VGAV
YCOEQ
FIE
FFWE
FFRSTW
FFRE
FFOE
CLK20
N302 VPC3230D
AISGND
FB1IN
VREF
GNDAI
VSUPAI
VIN4
VIN3
VIN2
VIN1
CIN
VOUT
VSUPF
ISGND
I2CSEL
VRT
GNDF
GNDPA
VSUPPA
LLC2
LLC1
VSUPLLC
GNDLLC
Y7
Y6
Y5
Y4
GNDY
VSUPY
Y3
Y2
Y1
Y0
ASGF-64
XTAL2
XTAL1
NC61
CLK5
VSTBY
FPDAT
VS
MSY/HS
FSY/HC
AVD
INTLC
VSUPSY
GNDSY
C0
C1
C2
C3
GNDC
VSUPC
C4
C5
C6
C7
G301 20.25MHz
C344 3.3p
C345 3.3p
C350 22uF
C351 100n
R340 47
R341 47
R342 47
R343 47
R344 47
R345 47
R346 47
R347 ?
C355 68n
C356 47n
C349 68n
C338 68n
C335 68n
R338 ?
C330 1.5n
C331 47n
GBE[0]
GBE[1]
GBE[2]
GBE[3]
GBE[4]
GBE[5]
GBE[6]
GBE[7]
GBE[0-7]
GGE[0]
GGE[1]
GGE[2]
GGE[3]
GGE[4]
GGE[5]
GGE[6]
GGE[7]
GGE[0-7]
R355 1K
R356 4.7K
V304 BC847AW
VD2_VSYNC
VD2_HSYNC
VD2_ACTIVE
VD2_FIELD
VD2_FIELD
VD2_ACTIVE
VD2_H
VD2_V
GND3
VD2_CLK
SCL_1
SDA_1
VD2_RST_N
VD2_OE_N
VD2_OE_N
+5V
L305 STBL2012-501
C304 10V 22uF
C308 100n
C313 10V 22uF
C316 100n
+3.3V
L306 STBL2012-501
C305 10V 22uF
C309 100n
C314 10V 22uF
C317 100n
CAUTION:The smallest filter capacitor must be closed to N401 pin!

Reduce EMI/current spikes suppress reflection.
Close to pin package-no via!

Minimize the trace length running into graphics input.
Don't run any digital or other high frequecy traces near it!

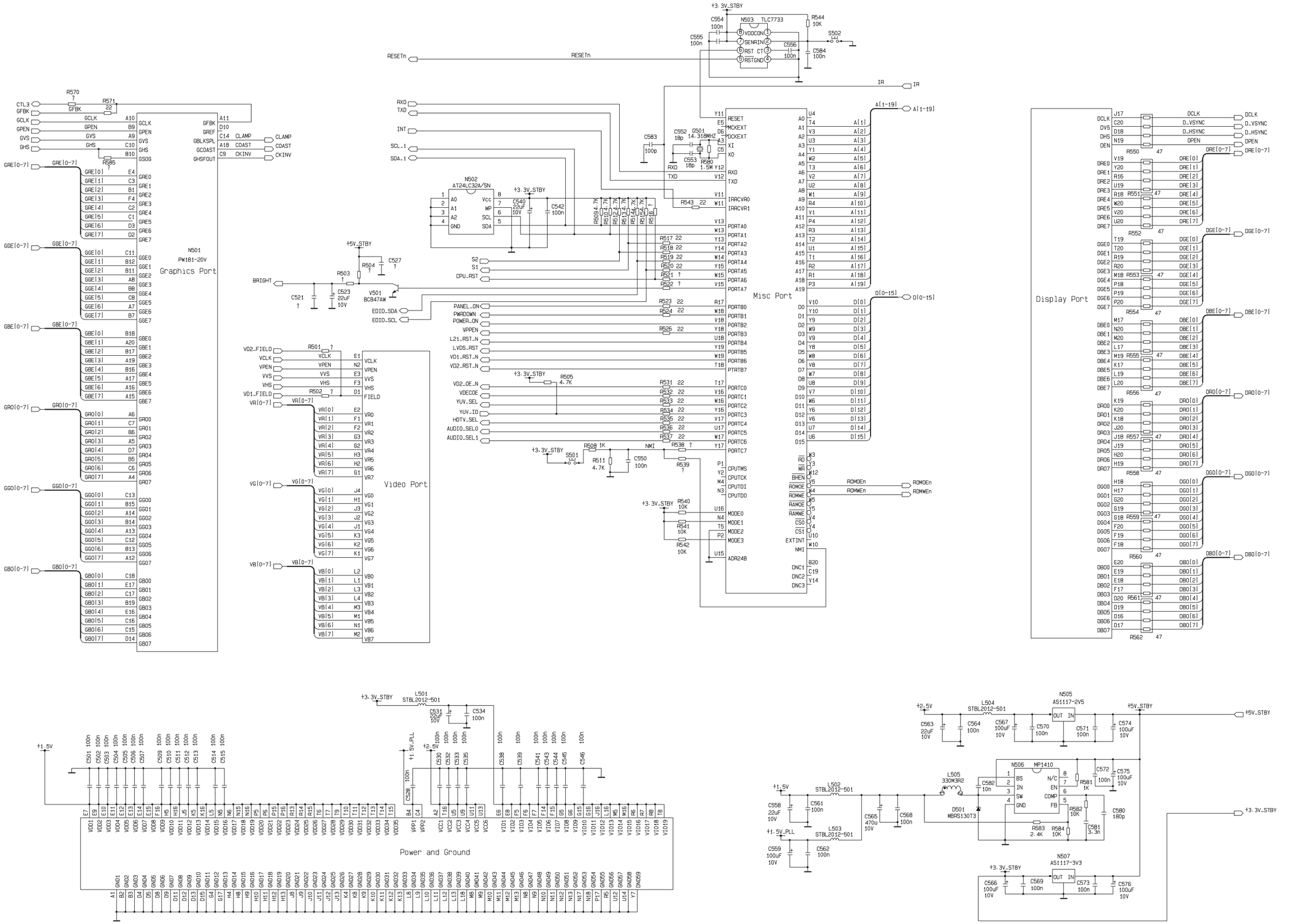
Don't place any digital or high frequecy traces near these component!

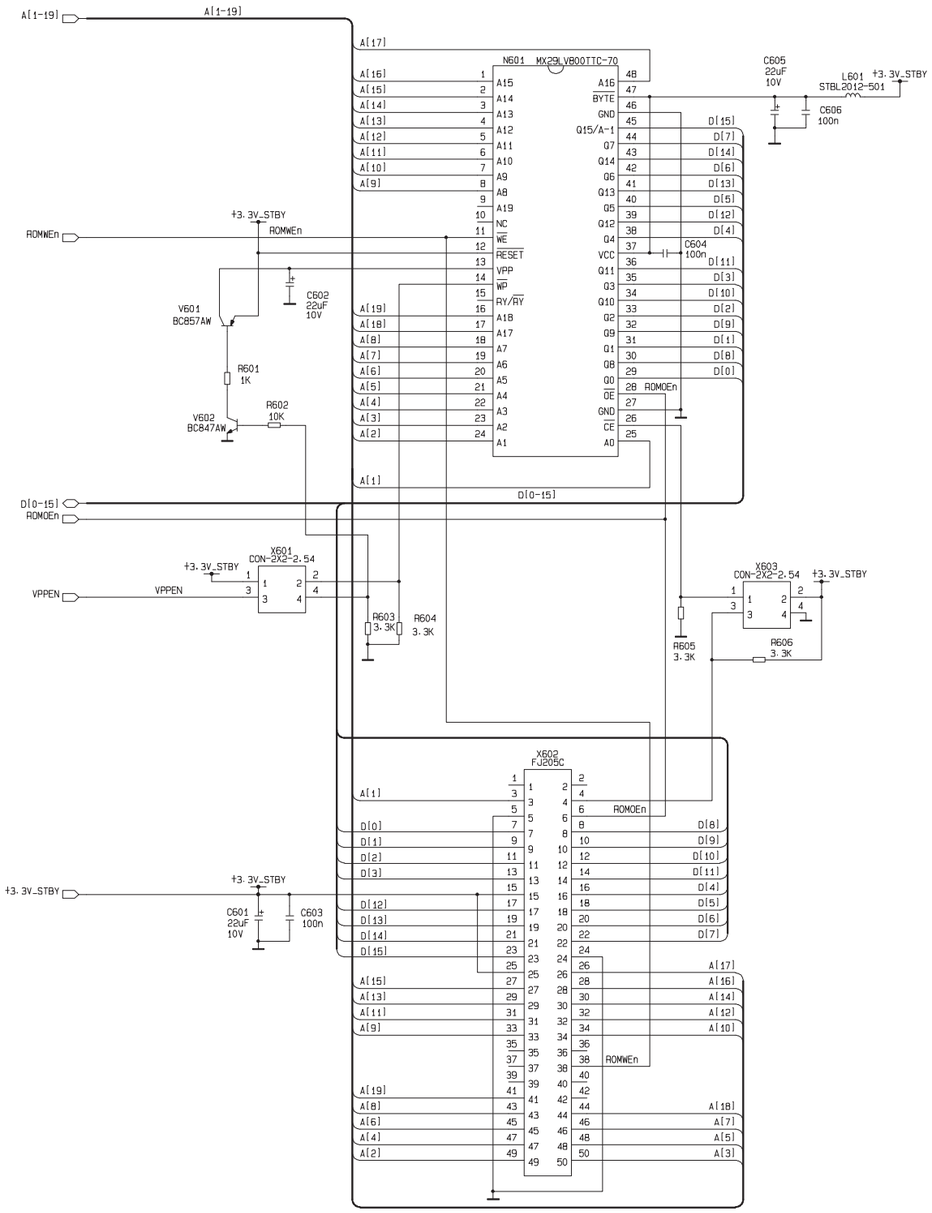
As close to FILT as possible!

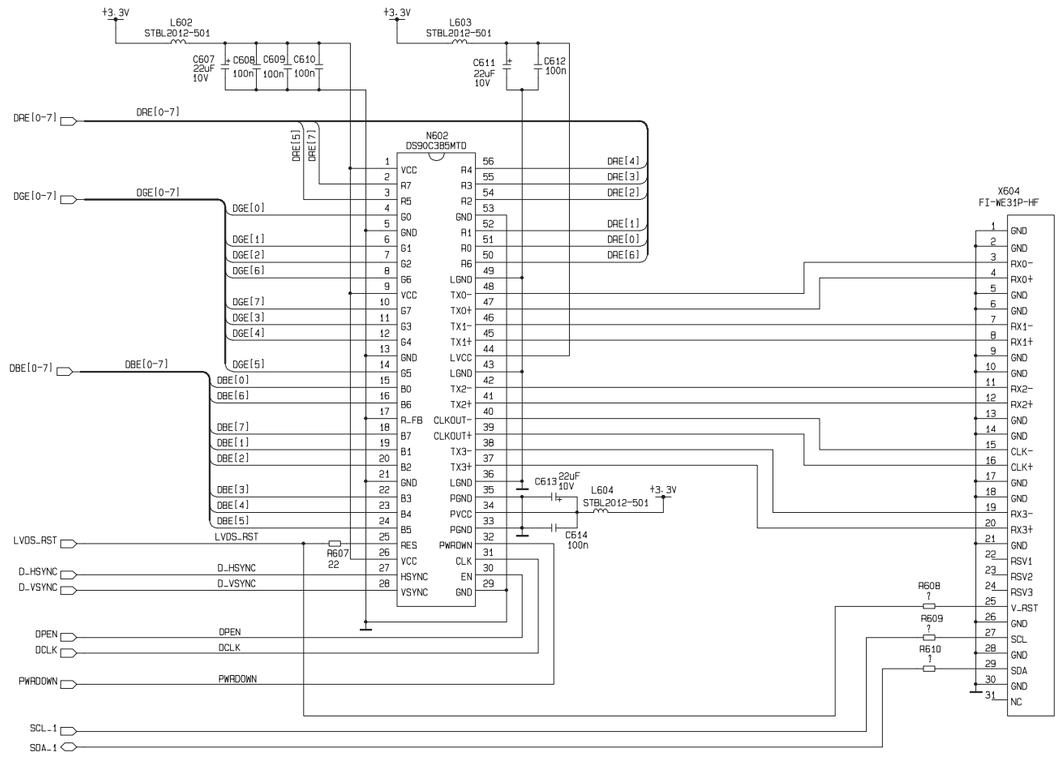
Avoid running any digital traces near the analog input!

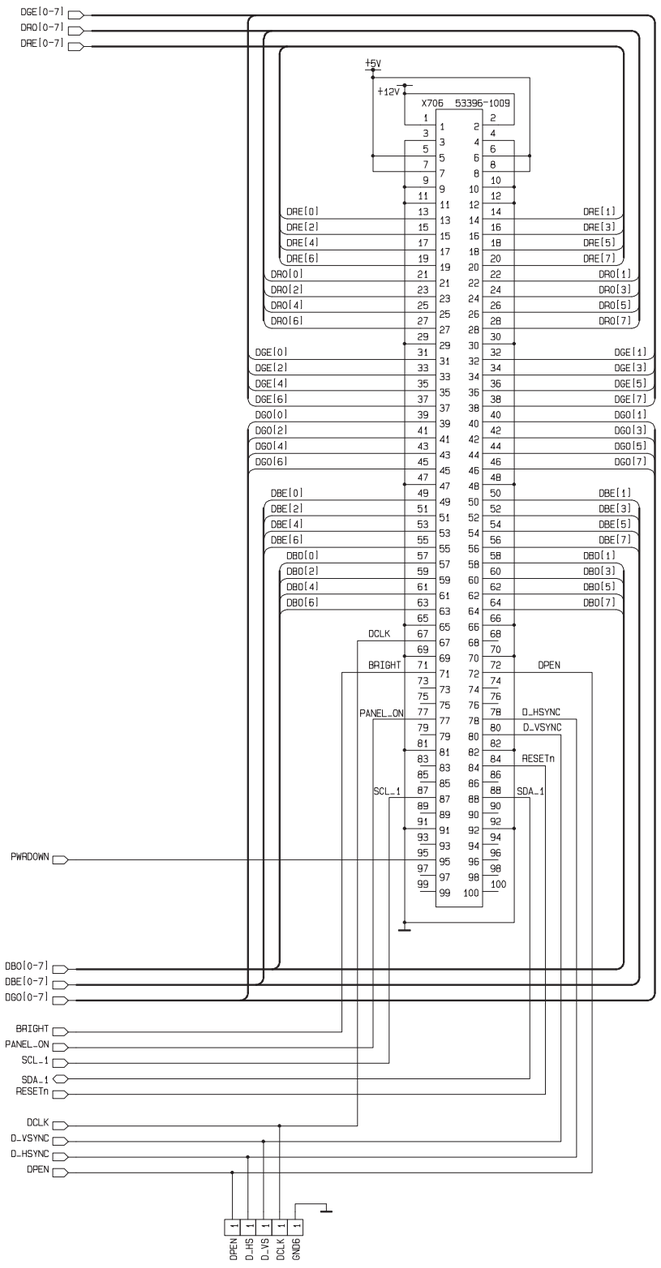
Analog power.

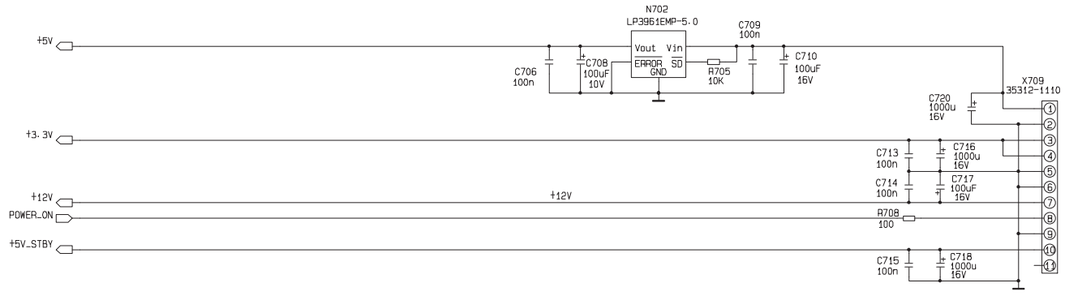
Output power.

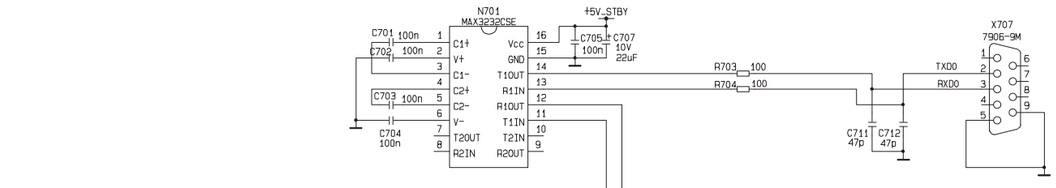

N501
PW181-20V
Graphics Port
Video Port
Misc Port
Display Port
N502
AT24LC32A/SN
N503
TLC7733
S501
S502
V501
BC847AW
L501
STBL2012-501
L502
STBL2012-501
L503
STBL2012-501
L504
STBL2012-501
L505
330M3R2
N505
AS1117-2V5
N506
MP1410
N507
AS1117-3V3
D501
MBRS130T3
Power and Ground
RESETn
IR
RXD
TXD
INT
SCL_1
SDA_1
S2
S1
CPU_RST
BRIGHT
EDID_SDA
EDID_SCL
PANEL_ON
PWRDOWN
POWER_ON
VPPEN
L21_RST_N
LVDS_RST
VD1_RST_N
VD2_RST_N
VD2_OE_N
VDECOE
YUV_SEL
YUV_ID
HDTV_SEL
AUDIO_SEL0
AUDIO_SEL1
NMI
CPUTMS
CPUTCK
CPUTDI
CPUTDO
MODE0
MODE1
MODE2
MODE3
ADR24B
EXTINT
ROMOEn
ROMWEn
A[1-19]
D[0-15]
CLAMP
COAST
CKINV
+3.3V_STBY
+5V_STBY
+1.5V
+2.5V
+1.5V_PLL
+3.3V_STBY

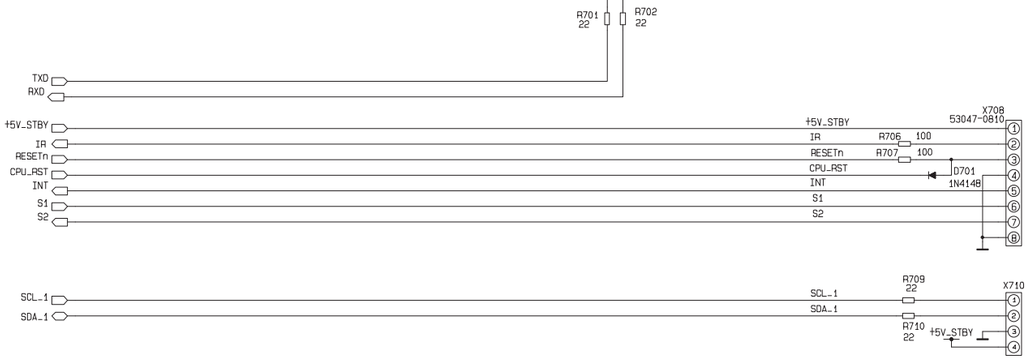

A[1-19]
N601 MX29LV800TTC-70
A[17]
A[16]
A[15]
A[14]
A[13]
A[12]
A[11]
A[10]
A[9]
A[8]
A[7]
A[6]
A[5]
A[4]
A[3]
A[2]
A[1]
A15
A14
A13
A12
A11
A10
A9
A8
NC
WE
RESET
VPP
WP
RY/BY
A18
A17
A7
A6
A5
A4
A3
A2
A1
A16
BYTE
GND
Q15/A-1
Q7
Q14
Q6
Q13
Q5
Q12
Q4
VCC
Q11
Q3
Q10
Q2
Q9
Q1
Q8
Q0
OE
GND
CE
A0
48
47
46
45
44
43
42
41
40
39
38
37
36
35
34
33
32
31
30
29
28
27
26
25
D[15]
D[7]
D[14]
D[6]
D[13]
D[5]
D[12]
D[4]
D[11]
D[3]
D[10]
D[2]
D[9]
D[1]
D[8]
D[0]
ROMOEn
C605 22uF 10V
C606 100n
C604 100n
+3.3V_STBY
L601 STBL2012-501
ROMWEn
V601 BC857AW
C602 22uF 10V
R601 1K
V602 BC847AW
R602 10K
D[0-15]
X601 CON-2X2-2.54
VPPEN
R603 3.3K
R604 3.3K
X603 CON-2X2-2.54
R605 3.3K
R606 3.3K
X602 FJ205C
C601 22uF 10V
C603 100n

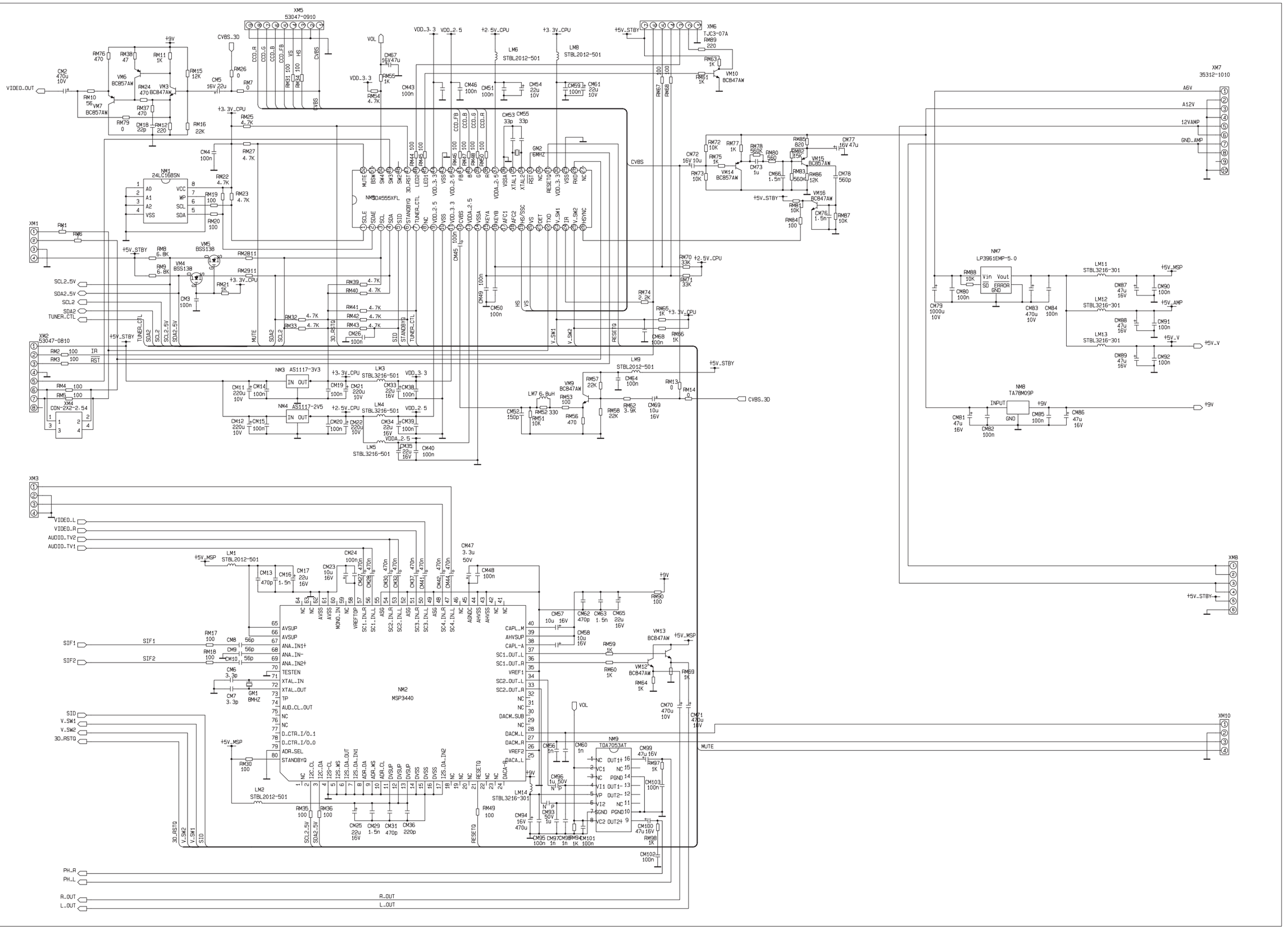

+3.3V
L602 STBL2012-501
L603 STBL2012-501
C607 22UF 10V
C608 100n
C609 100n
C610 100n
C611 22UF 10V
C612 100n
DRE[0-7]
DGE[0-7]
DBE[0-7]
N602 DS90C385MTD
VCC
R7
R5
G0
GND
G1
G2
G6
VCC
G7
G3
G4
GND
G5
B0
B6
R_FB
B7
B1
B2
GND
B3
B4
B5
RES
VCC
HSYNC
VSYNC
R4
R3
R2
GND
R1
R0
R6
LGND
TX0-
TX0+
TX1-
TX1+
LVCC
LGND
TX2-
TX2+
CLKOUT-
CLKOUT+
TX3-
TX3+
LGND
PGND
PVCC
PGND
PWRDOWN
CLK
EN
GND
X604 FI-WE31P-HF
RX0-
RX0+
RX1-
RX1+
RX2-
RX2+
CLK-
CLK+
RX3-
RX3+
RSV1
RSV2
RSV3
V_RST
SCL
SDA
NC
C613 22uF 10V
L604 STBL2012-501
C614 100n
LVDS_RST
R607 22
D_HSYNC
D_VSYNC
DPEN
DCLK
PWRDOWN
SCL_1
SDA_1
R608 ?
R609 ?
R610 ?

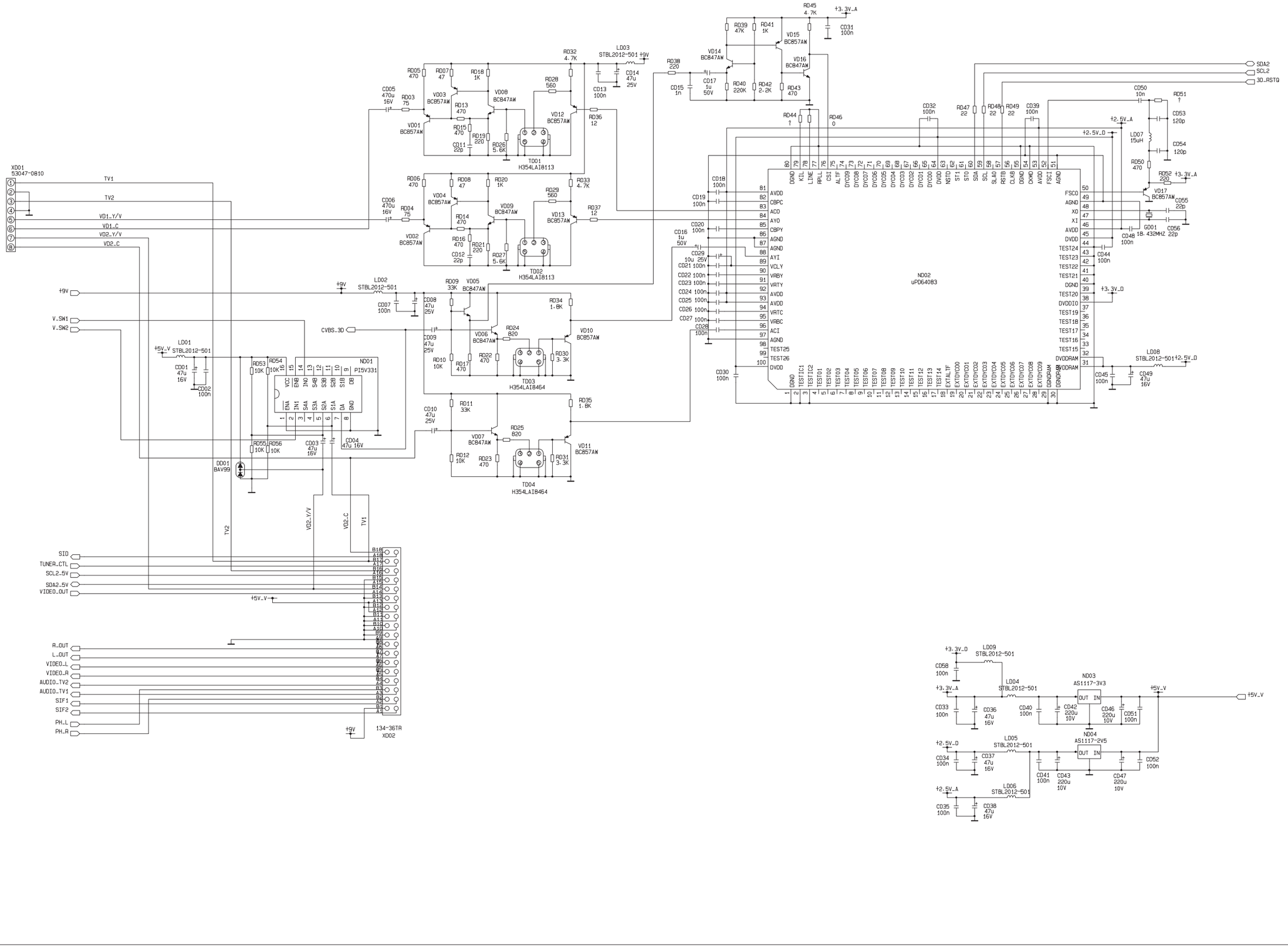

DGE[0~7]
DRO[0~7]
DRE[0~7]
+5V
+12V
X706 53396-1009
DRE[0]
DRE[1]
DRE[2]
DRE[3]
DRE[4]
DRE[5]
DRE[6]
DRE[7]
DRO[0]
DRO[1]
DRO[2]
DRO[3]
DRO[4]
DRO[5]
DRO[6]
DRO[7]
DGE[0]
DGE[1]
DGE[2]
DGE[3]
DGE[4]
DGE[5]
DGE[6]
DGE[7]
DGO[0]
DGO[1]
DGO[2]
DGO[3]
DGO[4]
DGO[5]
DGO[6]
DGO[7]
DBE[0]
DBE[1]
DBE[2]
DBE[3]
DBE[4]
DBE[5]
DBE[6]
DBE[7]
DBO[0]
DBO[1]
DBO[2]
DBO[3]
DBO[4]
DBO[5]
DBO[6]
DBO[7]
DCLK
BRIGHT
OPEN
PANEL_ON
D_HSYNC
D_VSYNC
RESETn
SCL_1
SDA_1
PWRDOWN
DBO[0~7]
DBE[0~7]
DGO[0~7]
BRIGHT
PANEL_ON
SCL_1
SDA_1
RESETn
DCLK
D_VSYNC
D_HSYNC
OPEN
OPEN
D_HS
D_VS
DCLK
GND6

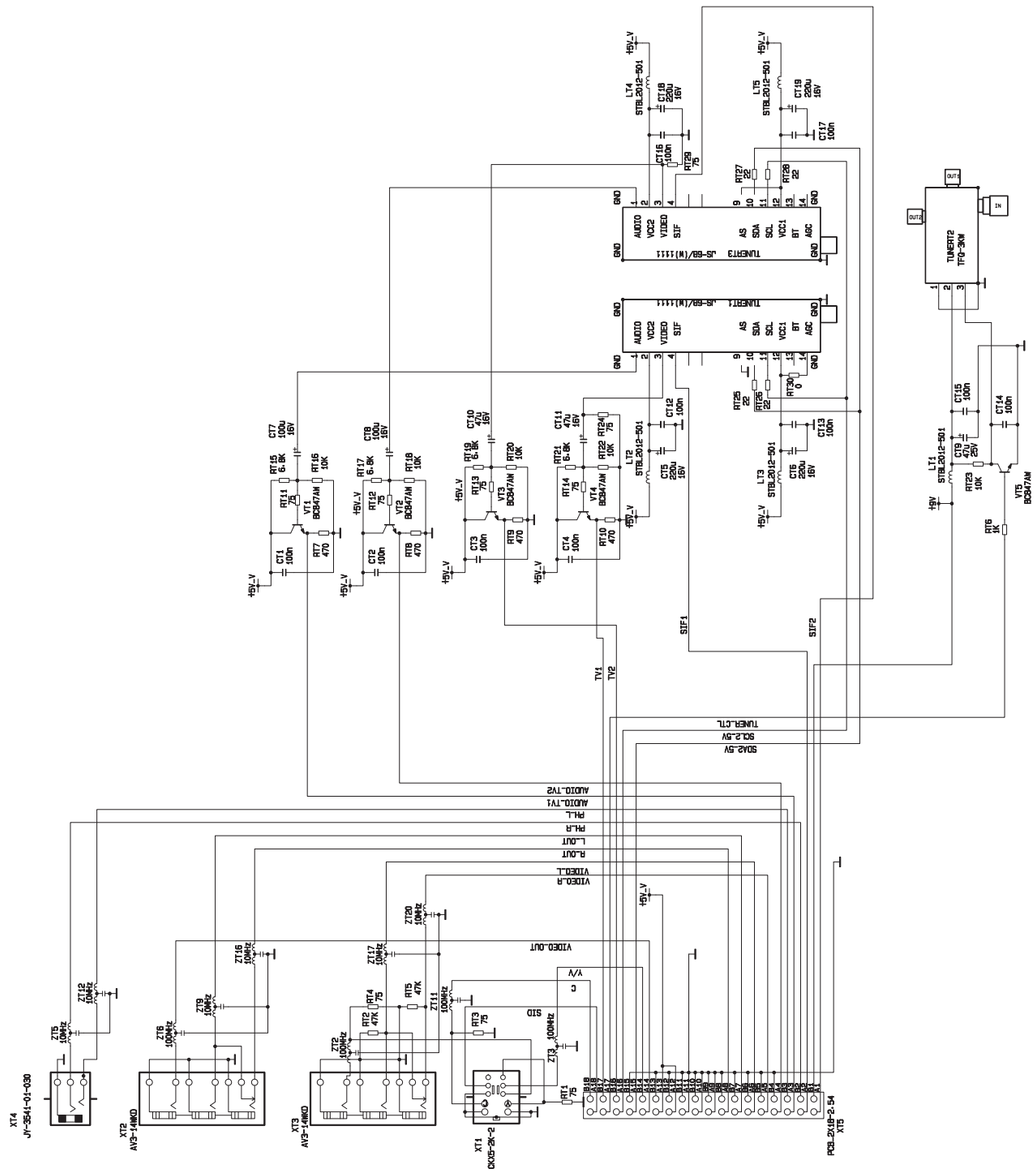

N702
LP3961EMP-5.0
Vout Vin
ERROR SD
GND
+5V
+3.3V
+12V
POWER_ON
+5V_STBY
C706 100n
C708 100uF 10V
C709 100n
C710 100uF 16V
R705 10K
X709 35312-1110
C720 1000u 16V
C713 100n
C716 1000u 16V
C714 100n
C717 100uF 16V
R708 100
C715 100n
C718 1000u 16V

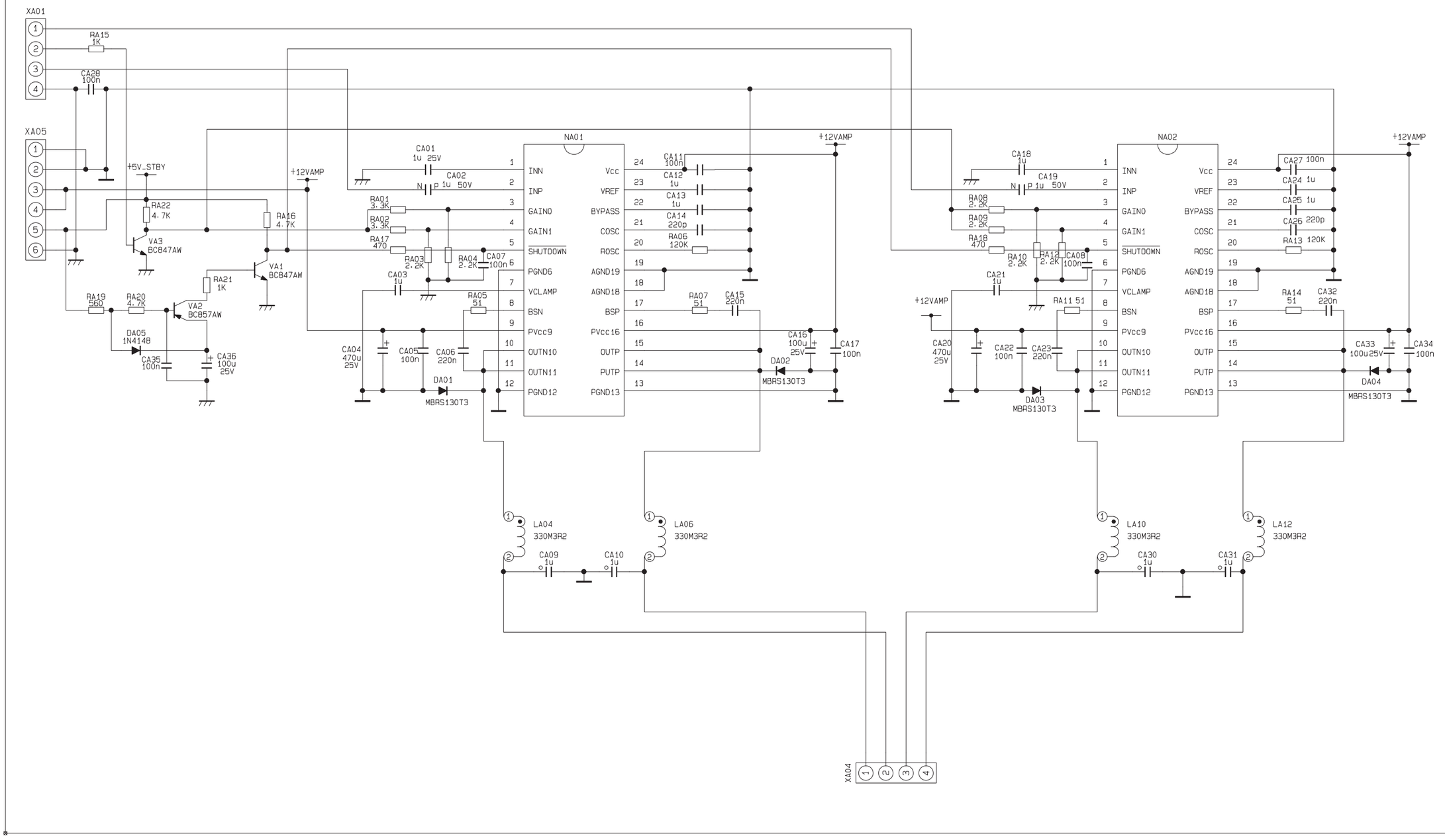

N701
MAX3232CSE
+5V_STBY
C701 100n
C702 100n
C703 100n
C704 100n
C705 100n
C707 10V 22uF
Vcc
GND
C1+
V+
C1-
C2+
C2-
V-
T2OUT
R2IN
T1OUT
R1IN
R1OUT
T1IN
T2IN
R2OUT
R703 100
R704 100
X707
7906-9M
TXD0
RXD0
C711 47p
C712 47p

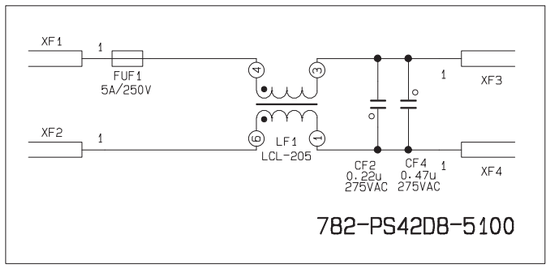

R701 22
R702 22
TXD
RXD
+5V_STBY
IR
RESETn
CPU_RST
INT
S1
S2
X708
53047-0810
R706 100
R707 100
D701
1N4148
SCL_1
SDA_1
R709 22
R710 22
X710

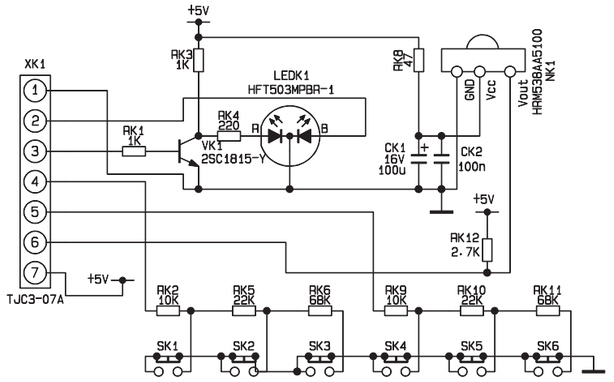

XM5
53047-0910
CVBS_3D
CCD_A
CCD_G
CCD_B
CCD_FB
VS
HS
CVBS
+9V
VIDEO_OUT
XM2
470u
10V
VM6
BC857AW
VM7
BC857AW
VM3
BC847AW
RM76 470
RM38 47
RM11 1K
RM15 12K
RM10 56
RM37 470
RM79 0
CM18 22p
RM12 220
RM16 22K
RM26 0
CM5 16V 22u
RM7 0
+3.3V_CPU
RM25 4.7K
CM4 100n
RM27 4.7K
NM1
24LC16BSN
RM22 4.7K
RM23 4.7K
RM19 100
RM20 100
NM5
TDA5555XFL
MUTE
BSW
SW4
SW3
SW2
3D_RST
LED2
LED1
VDD_3.3
VSS
VDD_2.5
FB
B
G
R
VDDA_2.5
VSSA
XTAL1
XTAL2
RST
NC
RESETQ
VDD_3.3
VSS
RXD
NC
SCLE
SDAE
SCL
SDA
STID
STANDBYQ
TUNER_CTL
NC
VDD_2.5
VSS
VDD_3.3
CVBS
VSSA
KEYA
KEYB
AFC1
AFC2
HS/SSC
VS
DET
TXD
V_SW1
IR
V_SW2
HSYNC
RM44 100
RM45 100
RM46 100
RM47 100
RM48 100
RM49 100
RM50 100
CM53 33p
CM55 33p
GM2
6MHZ
CVBS
VOL
VDD_3.3
VDD_2.5
+2.5V_CPU
+3.3V_CPU
+5V_STBY
LM6
STBL2012-501
LM8
STBL2012-501
CM67
16V 47u
RM55 1K
RM54 4.7K
CM43 100n
CM46 100n
CM51 100n
CM54 22u 10V
CM59 100n
CM61 22u 10V
RM67 100
RM68 100
XM6
TJC3-07A
RM89 220
RM63 1K
RM51 1K
VM10
BC847AW
XM7
35312-1010
A6V
A12V
12VAMP
GND_AMP
RM72 10K
RM77 1K
RM78 560K
RM80 560
RM85 820
RM82 15K
CM77 16V 47u
CM72 16V 10u
RM75 1K
RM73 10K
VM14
BC857AW
CM73 1u
VM15
BC857AW
CM66 1.5n
RM83 560K
RM86 12K
CM78 560p
VM16
BC847AW
RM81 10K
RM84 100
CM76 1.5n
RM87 10K
XM1
RM1
RM6
+5V_STBY
RM8 6.8K
RM9 6.8K
VM5
BSS138
VM4
BSS138
RM2811
RM2911
RM21 1K
+3.3V_CPU
CM3 100n
SCL2_5V
SDA2_5V
SCL2
SDA2
TUNER_CTL
RM39 4.7K
RM40 4.7K
RM41 4.7K
RM42 4.7K
RM43 4.7K
CM26 100n
RM32 4.7K
RM33 4.7K
RM70 33K
+2.5V_CPU
RM71 33K
CM49 100n
CM50 100n
HS
VS
RM74 2.2K
RM65 1K
+3.3V_CPU
CM68 100n
RM66 1K
XM2
53047-0810
RM2 100
RM3 100
IR
RST
RM4 100
RM5 100
XM4
CON-2X2-2.54
NM3
AS1117-3V3
IN
OUT
+3.3V_CPU
LM3
STBL3216-501
VDD_3.3
CM11 220u 10V
CM14 100n
CM19 100n
CM21 220u 10V
CM33 22u 16V
CM38 100n
NM4
AS1117-2V5
+2.5V_CPU
LM4
STBL3216-501
VDD_2.5
CM12 220u 10V
CM15 100n
CM20 100n
CM22 220u 10V
CM34 22u 16V
CM39 100n
VDDA_2.5
LM5
STBL3216-501
CM35 22u 16V
CM40 100n
LM9
STBL2012-501
+5V_STBY
RM57 22K
CM64 100n
RM13 0
RM14 0
CVBS_3D
LM7 6.8uH
CM52 150p
RM52 330
RM51 10K
RM53 100
VM9
BCB47AW
RM56 47Ω
RM58 22K
RM62 3.9K
CM69 10u 16V
NM7
LP3961EMP-5.0
RM88 10K
Vin
Vout
SD
ERROR
GND
CM79 1000u 10V
CM80 100n
CM83 470u 10V
CM84 100n
LM11
STBL3216-301
+5V_MSP
CM87 47u 16V
CM90 100n
LM12
STBL3216-301
+5V_AMP
CM88 47u 16V
CM91 100n
LM13
STBL3216-301
+5V_V
CM89 47u 16V
CM92 100n
NM8
TA78M09P
INPUT
+9V
GND
CM81 47u 16V
CM82 100n
CM85 100n
CM86 47u 16V
XM3
VIDEO_L
VIDEO_R
AUDIO_TV2
AUDIO_TV1
LM1
STBL2012-501
+5V_MSP
CM13 470p
CM16 1.5n
CM17 22u 16V
CM24 1000u
CM23 10u 16V
CM27 470n 16
CM28 470n 16
CM30 470n 16
CM32 470n 16
CM37 470n 16
CM41 470n 16
CM42 470n 16
CM44 470n 16
CM47 3.3u 50V
CM48 100n
+9V
RM90 100
CM57 10u 16V
CM62 470p
CM63 1.5n
CM65 22u 16V
CM58 10u 16V
RM59 1K
RM60 1K
VM13
BC847AW
VM12
BC847AW
RM64 1K
RM69 1K
+5V_MSP
CM70 470u 10V
CM71 470u 10V
SIF1
SIF2
RM17 100
RM18 100
CM8 56p
CM9 56p
CM10 56p
CM6 3.3p
CM7 3.3p
GM1
6MHZ
NM2
MSP3440
AVSUP
ANA_IN1+
ANA_IN-
ANA_IN2+
TESTEN
XTAL_IN
XTAL_OUT
TP
AUD_CL_OUT
D_CTR_I/O_1
D_CTR_I/O_0
ADR_SEL
STANDBYQ
I2C_CL
I2C_DA
I2S_CL
I2S_WS
I2S_DA_OUT
I2S_DA_IN1
ADR_DA
ADR_WS
ADR_CL
DVSUP
DVSS
I2S_DA_IN2
RESETQ
DACA_R
CAPL_M
AHVSUP
CAPL_A
SC1_OUT_L
SC1_OUT_R
VREF1
SC2_OUT_L
SC2_OUT_R
DACM_SUB
DACM_L
DACM_R
VREF2
DACA_L
SID
V_SW1
V_SW2
3D_RSTQ
+5V_MSP
RM30 100
LM2
STBL2012-501
RM35 100
RM36 100
CM25 22u 16V
CM29 1.5n
CM31 470p
CM36 220p
RM49 100
NM9
TDA7053AT
CM56 1n
CM60 1n
CM96 1u 50V
CM93 50V 1u
LM14
STBL3216-301
CM94 16V 470u
CM95 100n
CM97 1n
CM98 1n
RM94 1K
CM101 100n
CM99 47u 16V
RM97 1K
CM103 100n
CM100 47u 16V
RM98 1K
CM102 100n
XM8
+5V_STBY
XM10
MUTE
PH_R
PH_L
R_OUT
L_OUT

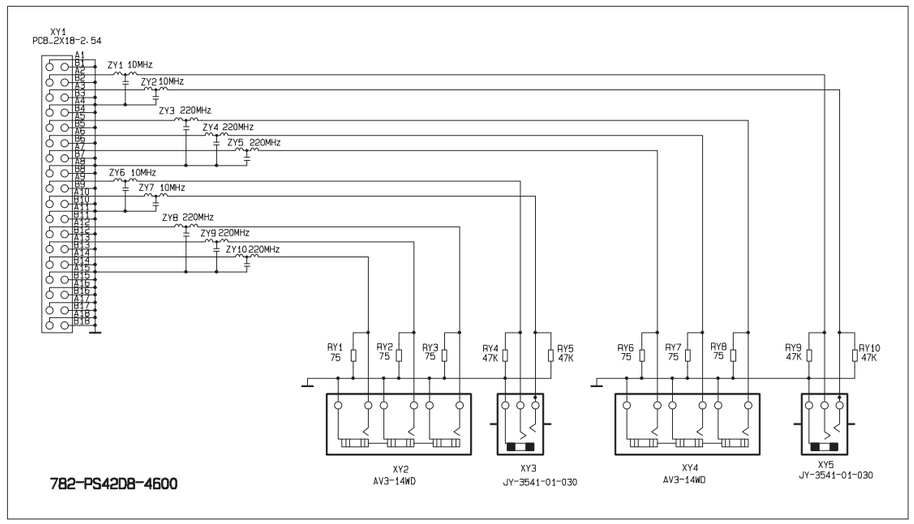

XD01
53047-0810
TV1
TV2
VD1_Y/V
VD1_C
VD2_Y/V
VD2_C
+9V
V_SW1
V_SW2
CVBS_3D
+5V_V
LD01
STBL2012-501
CD01
47u
16V
CD02
100n
ND01
PI5V331
RD53
10K
RD54
10K
RD55
10K
RD56
10K
DD01
BAV99
LD02
STBL2012-501
CD07
100n
CD08
47u
25V
CD09
47u
25V
CD10
47u
25V
CD03
47u
16V
CD04
47u 16V
VD05
BC847AW
VD06
BC847AW
VD07
BC847AW
RD09
33K
RD10
10K
RD11
33K
RD12
10K
RD24
820
RD25
820
RD22
470
RD23
470
RD34
1.8K
RD35
1.8K
RD30
3.3K
RD31
3.3K
VD10
BC857AW
VD11
BC857AW
TD03
H354LAI8464
TD04
H354LAI8464
LD03
STBL2012-501
+9V
CD14
47u
25V
CD13
100n
RD32
4.7K
RD05
470
RD07
47
RD18
1K
RD03
75
CD05
470u
16V
VD03
BC857AW
VD08
BC847AW
VD01
BC857AW
RD13
470
RD15
470
RD19
220
CD11
22p
RD26
5.6K
RD28
560
RD36
12
VD12
BC857AW
TD01
H354LAI8113
RD06
470
RD08
47
RD20
1K
RD04
75
CD06
470u
16V
VD04
BC847AW
VD09
BC847AW
VD02
BC857AW
RD14
470
RD16
470
RD21
220
CD12
22p
RD27
5.6K
RD29
560
RD33
4.7K
RD37
12
VD13
BC857AW
TD02
H354LAI8113
RD38
220
CD15
1n
CD17
1u
50V
RD45
4.7K
+3.3V_A
CD31
100n
RD39
47K
RD41
1K
RD40
220K
RD42
2.2K
RD43
470
VD14
BC847AW
VD15
BC857AW
VD16
BC847AW
RD44
?
RD46
0
ND02
uPD6408B3
CD18
100n
CD19
100n
CD20
100n
CD16
1u
50V
CD29
10u 25V
CD21
100n
CD22
100n
CD23
100n
CD24
100n
CD25
100n
CD26
100n
CD27
100n
CD28
100n
CD30
100n
CD32
100n
CD39
100n
RD47
22
RD48
22
RD49
22
+2.5V_A
+2.5V_D
LD07
15uH
CD50
10n
RD51
?
CD53
120p
CD54
120p
RD50
470
RD52
220
VD17
BC857AW
CD55
22p
CD56
22p
G001
18.432MHZ
CD48
100n
CD44
100n
+3.3V_D
LD08
STBL2012-501
CD45
100n
CD49
47u
16V
SDA2
SCL2
3D_RSTQ
SIO
TUNER_CTL
SCL2_5V
SDA2_5V
VIDEO_OUT
A_OUT
L_OUT
VIDEO_L
VIDEO_R
AUDIO_TV2
AUDIO_TV1
SIF1
SIF2
PH_L
PH_R
134-36TR
XD02
+3.3V_D
LD09
STBL2012-501
CD58
100n
LD04
STBL2012-501
CD33
100n
CD36
47u
16V
CD40
100n
ND03
AS1117-3V3
CD42
220u
10V
CD46
220u
10V
CD51
100n
+5V_V
ND04
AS1117-2V5
LD05
STBL2012-501
+2.5V_D
CD34
100n
CD37
47u
16V
CD41
100n
CD43
220u
10V
CD47
220u
10V
CD52
100n
LD06
STBL2012-501
+2.5V_A
CD35
100n
CD38
47u
16V


TUNER_CTL
SCL2_5V
SDA2_5V
AUDIO_TV2
AUDIO_TV1
PALL
PALR
L_OUT
R_OUT
VIDEO_L
VIDEO_R
VIDEO_OUT
SIF1
SIF2
TV1
TV2
SCL
SDA
+5V_V
+9V
TUNER73 JS-6B/(M)1111
TUNER72 TF9-3KM
AUDIO
VCC2
VIDEO
SIF
AS
SDA
SCL
VCC1
BT
AGC
GND
L74 STBL2012-601
L75 STBL2012-601
L72 STBL2012-601
L73 STBL2012-601
L71 STBL2012-601
CT16 100n
CT17 100n
CT18 220u 16V
CT19 220u 16V
CT1 100n
CT2 100n
CT3 100n
CT4 100n
CT5 220u 16V
CT6 220u 16V
CT7 100u 16V
CT8 100u 16V
CT9 220u 16V
CT10 470 16V
CT11 470 16V
CT12 100n
CT13 100n
CT14 100n
CT15 100n
RT7 470
RT8 470
RT9 470
RT10 470
RT11 75
RT12 75
RT13 75
RT14 75
RT15 6.8K
RT16 10K
RT17 6.8K
RT18 10K
RT19 6.8K
RT20 10K
RT21 6.8K
RT22 10K
RT23 10K
RT24 75
RT25 22
RT26 22
RT27 22
RT28 22
RT29 75
RT30 0
VT1 BC547AM
VT2 BC547AM
VT3 BC547AM
VT4 BC547AM
VT5 BC547AM
XT1 DC02-2K-2
XT2 AV3-14MKD
XT3 AV3-14MKD
XT4 JY-3541-01-030
XT5 PCB-2X18-2.54
Z11 100MHz
Z12 100MHz
Z13 100MHz
Z14 100MHz
Z15 100MHz
Z16 100MHz
Z17 100MHz
Z18 100MHz
Z19 100MHz
Z20 100MHz
RT1 75
RT2 75
RT3 75
RT4 75
RT5 47K
RT6 47K


XA01
XA05
XA04
RA15 1K
CA28 100n
+5V_STBY
+12VAMP
RA22 4.7K
RA16 4.7K
VA3 BC847AW
VA1 BC847AW
VA2 BC857AW
RA21 1K
RA19 560
RA20 4.7K
DA05 1N4148
CA35 100n
CA36 100u 25V
NA01
CA01 1u 25V
CA02 NP 1u 50V
RA01 3.3K
RA02 3.3K
RA17 470
RA03 2.2K
RA04 2.2K
CA07 100n
CA03 1u
RA05 51
CA04 470u 25V
CA05 100n
CA06 220n
DA01 MBRS130T3
INN
INP
GAIN0
GAIN1
SHUTDOWN
PGND6
VCLAMP
BSN
PVcc9
OUTN10
OUTN11
PGND12
Vcc
VREF
BYPASS
COSC
ROSC
AGND19
AGND18
BSP
PVcc16
OUTP
PUTP
PGND13
CA11 100n
CA12 1u
CA13 1u
CA14 220p
RA06 120K
RA07 51
CA15 220n
CA16 100u 25V
CA17 100n
DA02 MBRS130T3
NA02
CA18 1u
CA19 NP 1u 50V
RA08 2.2K
RA09 2.2K
RA18 470
RA10 2.2K
RA12 2.2K
CA08 100n
CA21 1u
RA11 51
CA20 470u 25V
CA22 100n
CA23 220n
DA03 MBRS130T3
CA27 100n
CA24 1u
CA25 1u
CA26 220p
RA13 120K
RA14 51
CA32 220n
CA33 100u 25V
CA34 100n
DA04 MBRS130T3
LA04 330M3R2
LA06 330M3R2
LA10 330M3R2
LA12 330M3R2
CA09 1u
CA10 1u
CA30 1u
CA31 1u
+12VAMP


XF1
1
FUF1
5A/250V
XF2
1
LF1
LCL-205
CF2
0.22u
275VAC
CF4
0.47u
275VAC
1
XF3
XF4
782-PS42D8-5100


+5V
XK1
TJC3-07A
RK3
1K
LEDK1
HFT503MPBA-1
RK8
47
Vout
GND
Vcc
HRM538AA5100
NK1
RK1
1K
RK4
220
VK1
2SC1815-Y
CK1
16V
100u
CK2
100n
RK12
2.7K
RK2
10K
RK5
22K
RK6
68K
RK9
10K
RK10
22K
RK11
68K
SK1
SK2
SK3
SK4
SK5
SK6


XY1
PCB_2X18-2.54
ZY1 10MHz
ZY2 10MHz
ZY3 220MHz
ZY4 220MHz
ZY5 220MHz
ZY6 10MHz
ZY7 10MHz
ZY8 220MHz
ZY9 220MHz
ZY10 220MHz
RY1
75
RY2
75
RY3
75
RY4
47K
RY5
47K
RY6
75
RY7
75
RY8
75
RY9
47K
RY10
47K
XY2
AV3-14WD
XY3
JY-3541-01-030
XY4
AV3-14WD
XY5
JY-3541-01-030
782-PS42D8-4600